

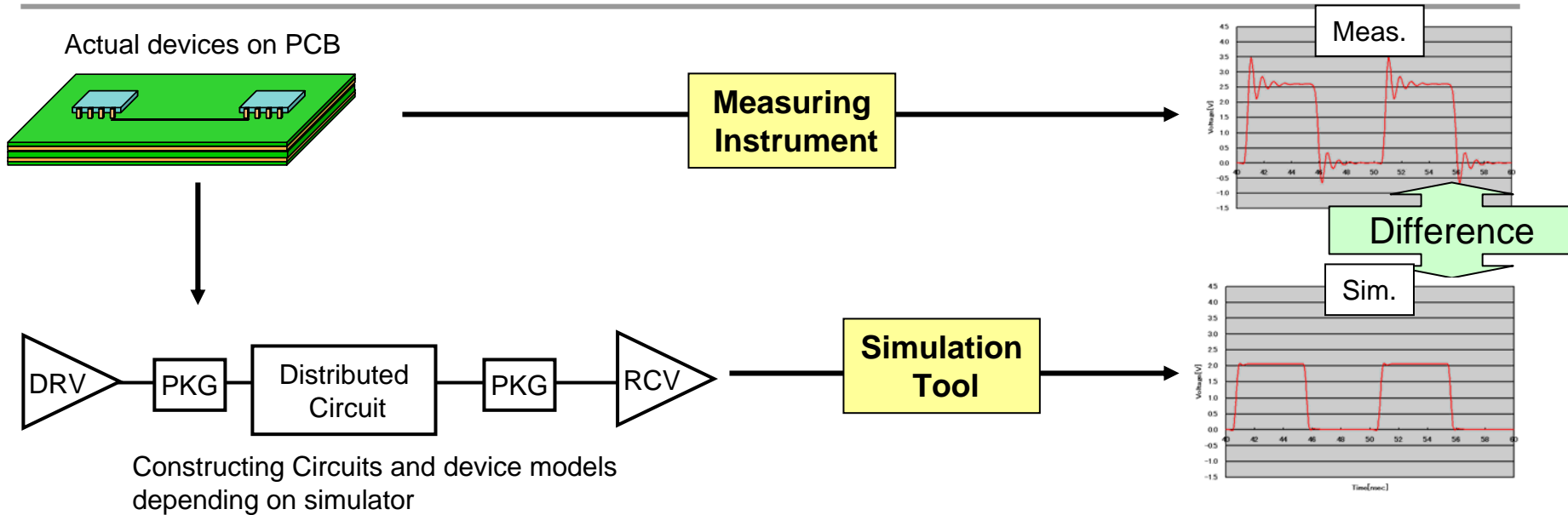
IBIS Quality Activities
in JEITA EDA WG

2007/09/14
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What's the "Quality"?

- There are many view points for "Quality"
- In the Dictionary, "Quality" means that "standard of **something** when it is compared to **other things like it**".
- At first, we define the "Quality" in this activity as "standard of **simulation result with the device EDA models** when it is compared to **the measurement result with the device**"
- But, this definition is very difficult...

The difference between Meas. and Simulation ?

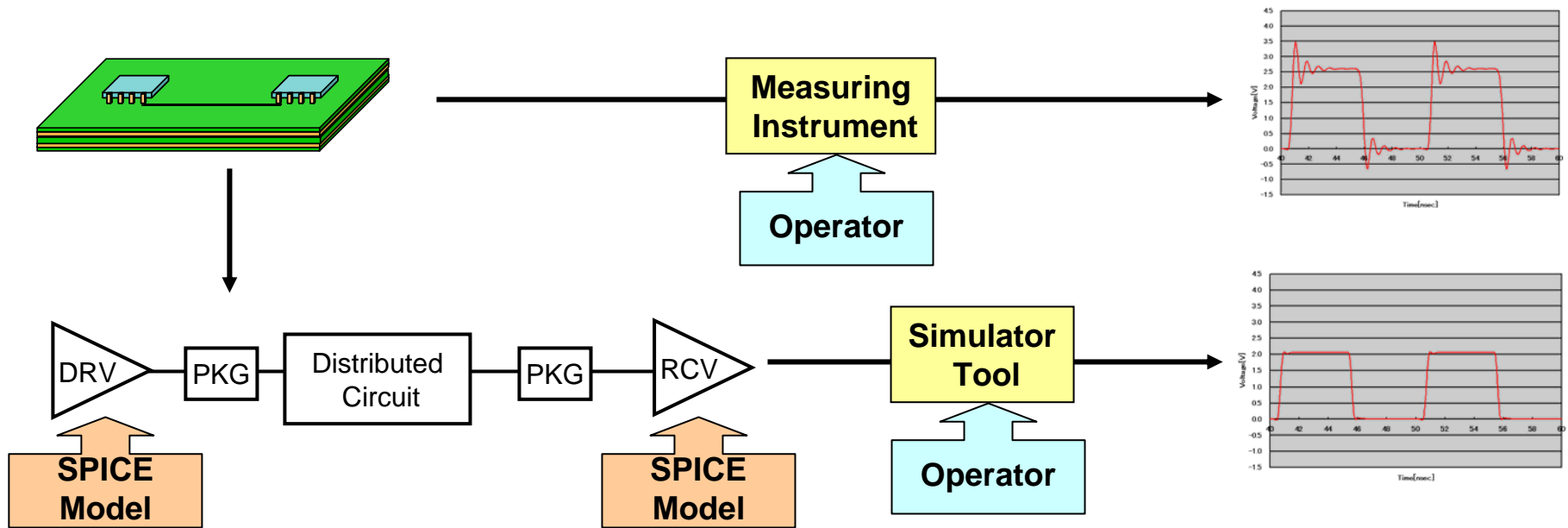


Simulation result does not necessary agree with measuring waveform.

What causes this difference??

There are so many reasons...

What causes this difference?



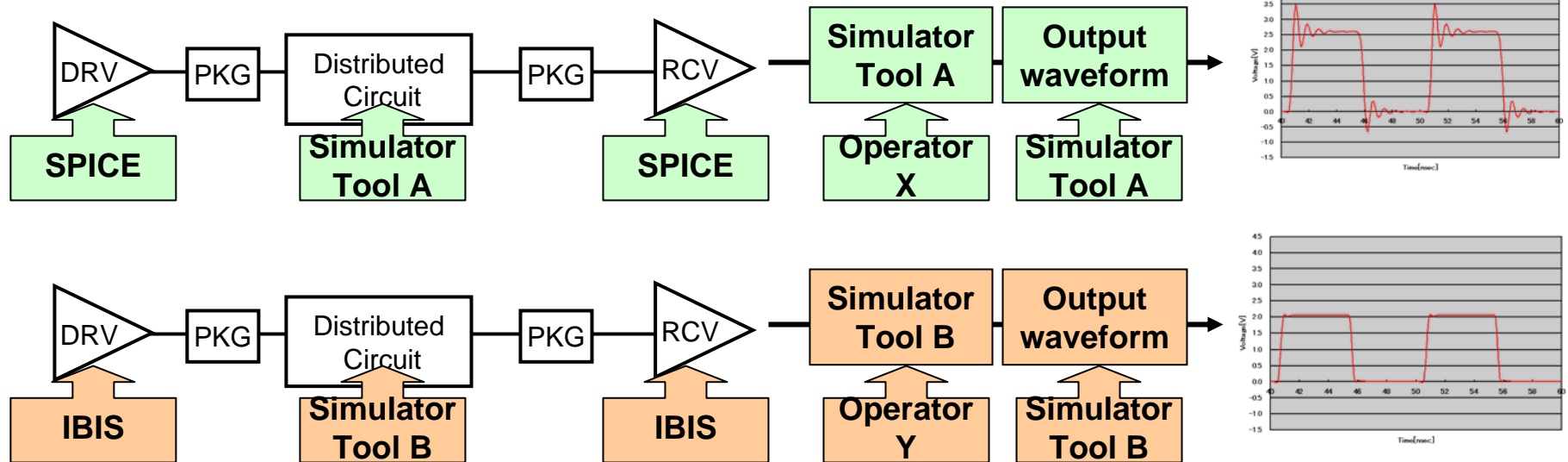
1. The problem on the Measuring instrument...
2. The operator cannot use Measuring instrument well...
3. SPICE Model accuracy is too poor...
4. Simulation tools with SPICE Model cannot simulate accurately...
5. The operator cannot use Simulation tools well...
(including not knowing how to set it up rightly)

*1,2 are dependent on the measuring matter,
3,4,5 are dependent on semi-conductor vendors internal.
JEITA doesn't focus on them as the "Quality".
Please, let the semi-conductor vendors do well.*

The next focus on the "Quality"

- We redefine the "Quality" in this activity as "standard of **the simulation result using IBIS models** when it is compared to **that using SPICE models**"
- Unfortunately, even this definition has some problems...
- The discrepancy between IBIS and SPICE waveform results are caused by not only **the different model** (IBIS and SPICE) but also **different simulators , operators , setting up the environment , viewing tool of waveform depending on the simulator** (ex. time step control for viewing) .

What should we focus on for the "IBIS Quality"?



When two waveforms are different, can you assert that these differences are caused by the distinctions of IBIS and SPICE model?

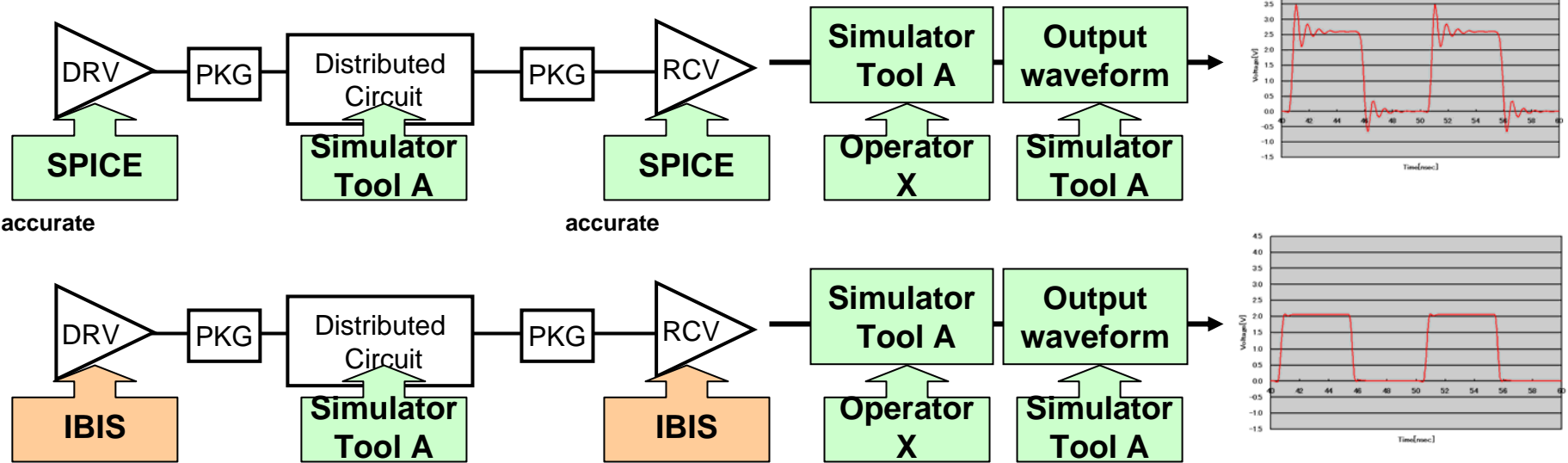
Sometimes Yes, actually we don't know.

When semiconductor vendors receive the question from customers, they must confirm their customer's simulation environment and reappear the customer's problems with same tools...

JEITA consider that "IBIS Quality" is NOT only IBIS Model accuracy itself.

What should we focus on for the "IBIS Quality"?

JEITA activities for "IBIS Quality" (1)



Assumption:

- (1) Operator is fixed; besides that operator has the best ability.
- (2) Simulator is fixed; besides that simulator can calculate circuits using IBIS and SPICE accurately.

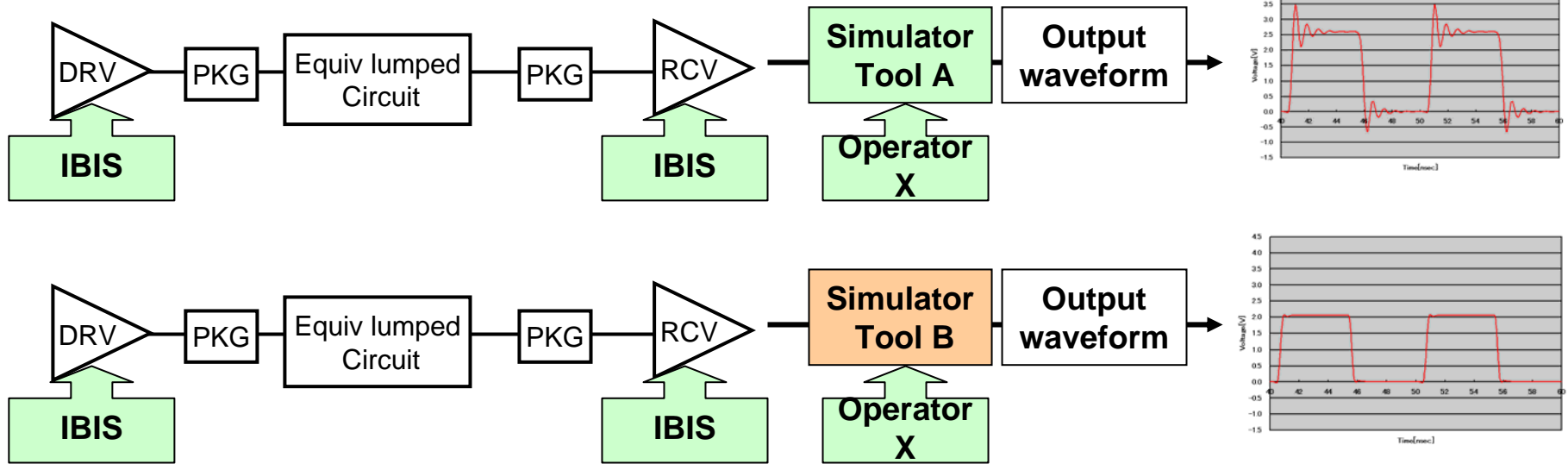
==> The difference is caused by the distinction of IBIS and SPICE.

What's more assumption: (3) SPICE is accurate

==> IBIS is Wrong!!

*Task Group in JEITA study this...
"IBIS Guide for the Japanese Engineer"*

JEITA activities for "IBIS Quality"(2)



Assumption:

- (1) Operator is fixed; besides that operator has the best ability.
- (2) IBIS is accurate

Condition:

- (1) Changing "distributed circuit" to equivalent "lumped circuit" using LCR
- (2) using same viewing tool (like EXCEL)

*Is the simulation result calculated by different simulators same??
→ JEITA studies this matter in the activity.*

The steps in this activity

- 1. Considering test circuits for "IBIS Quality".
Single / Differential model
simple 50Ohm resistance load
/ with complex transmission line**
- 2. Cooperating with the EDA vendors for this activity**
- 3. Selecting IBIS Models from JEITA members**

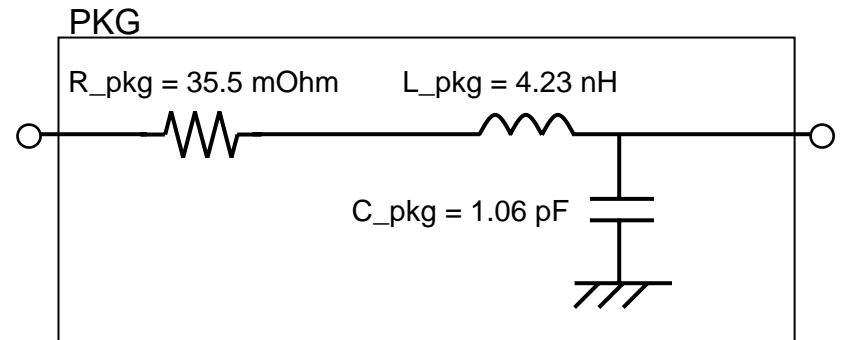
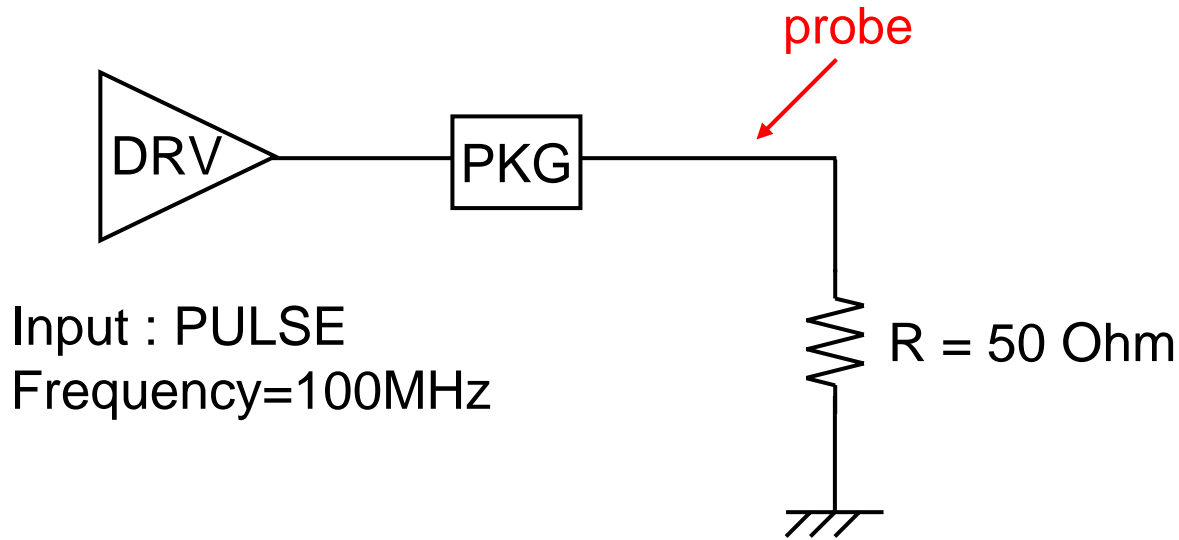
Single-ended

Model type
Input/Output

Voltage range
2.6V

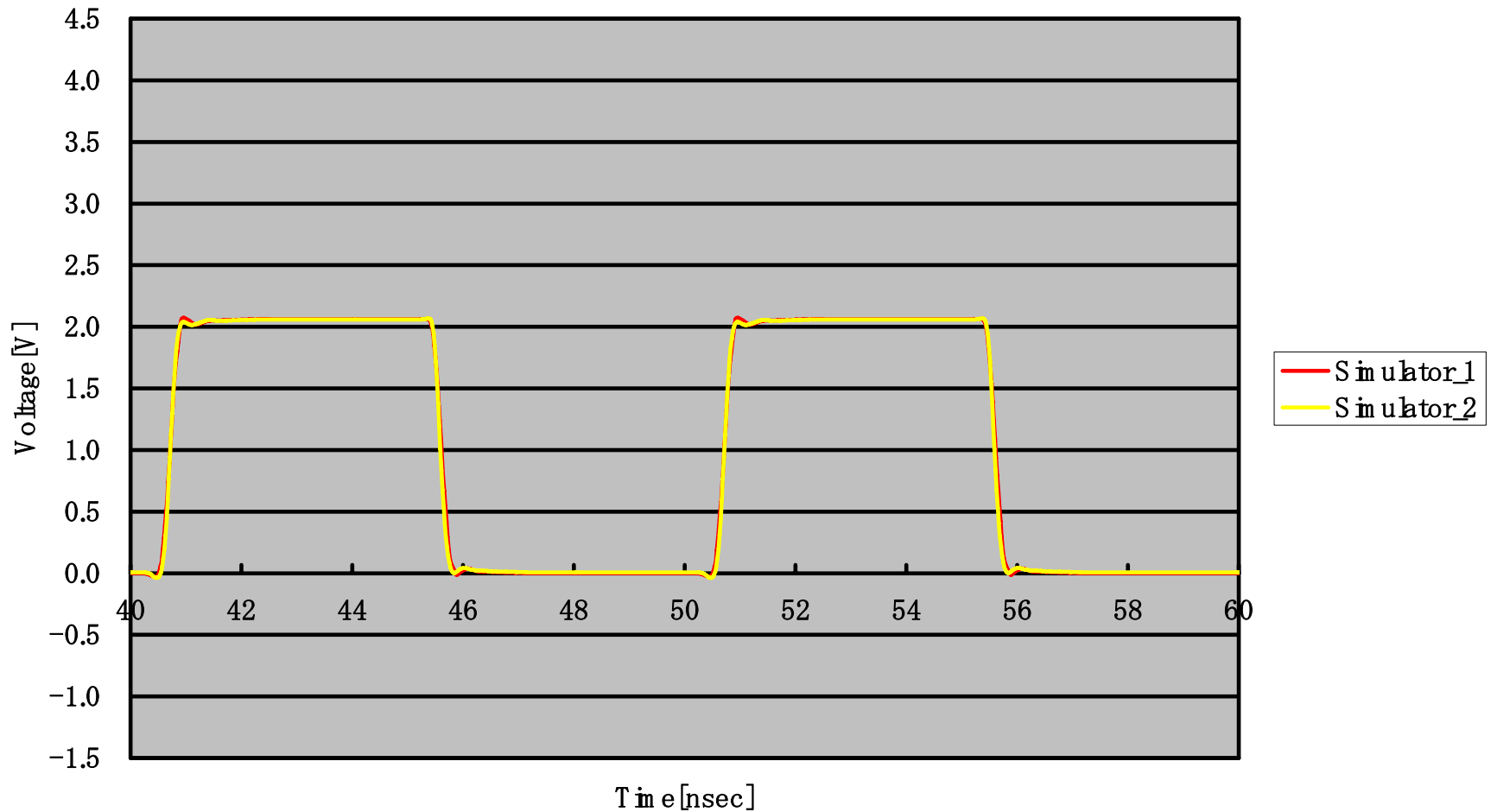
Used V-T data (ramp/waveform)
Golden Waveform

Evaluation circuit 1



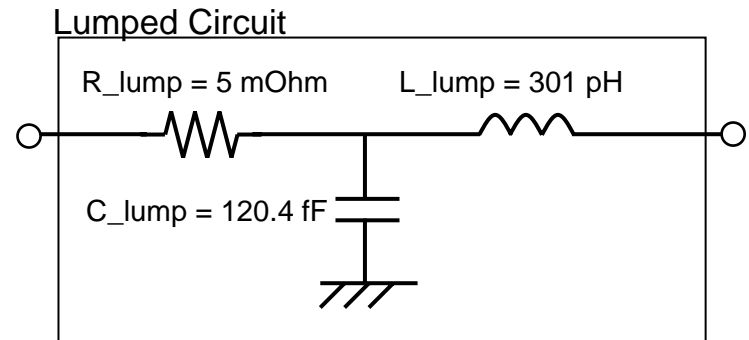
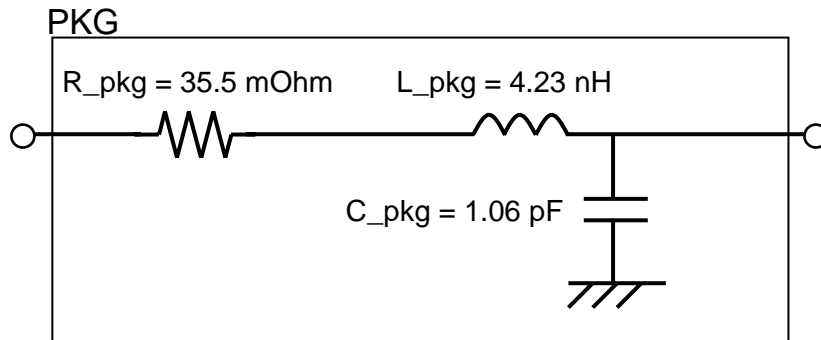
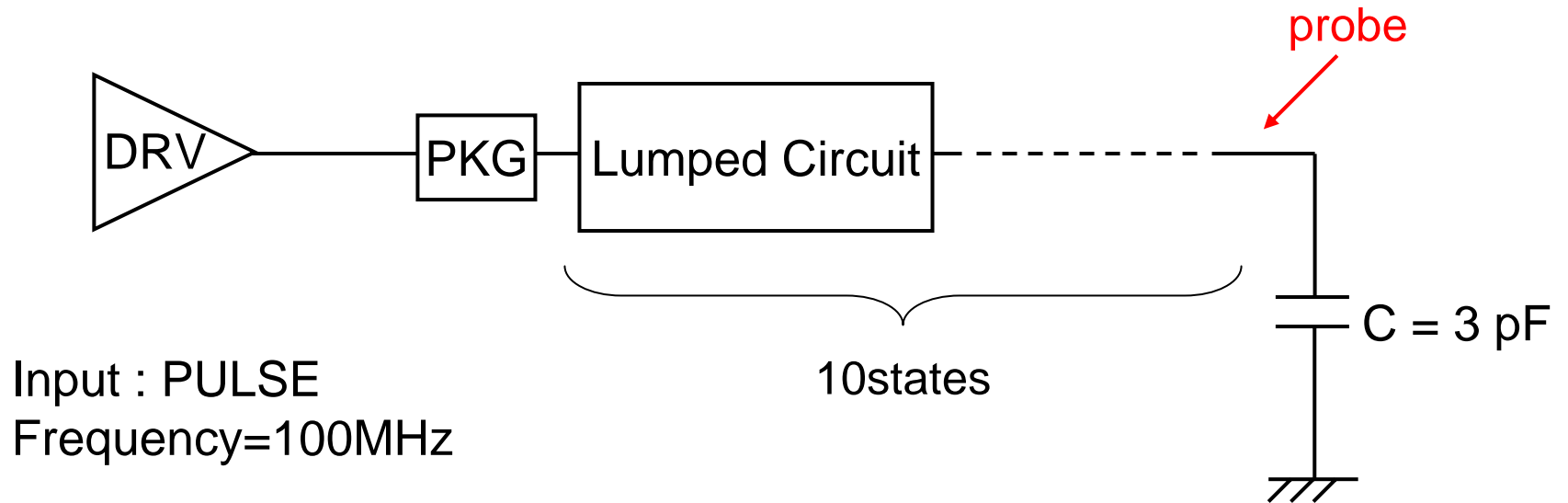
Result

Resistance termination (GND)



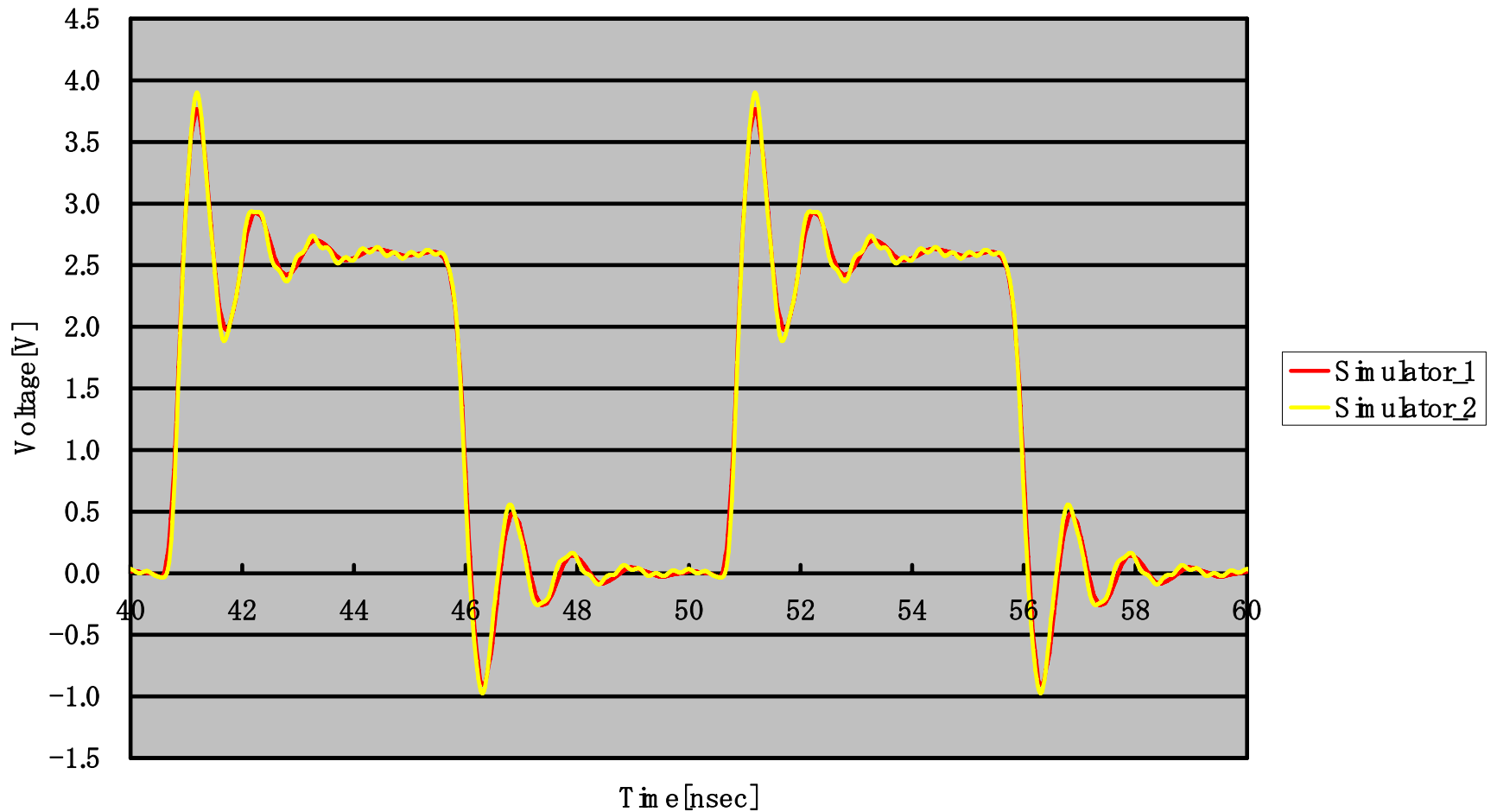
time adjustment

Evaluation circuit 2



Result

Transmission line (multistage lumped circuit $N=10$)+Capacitance termination



time adjustment

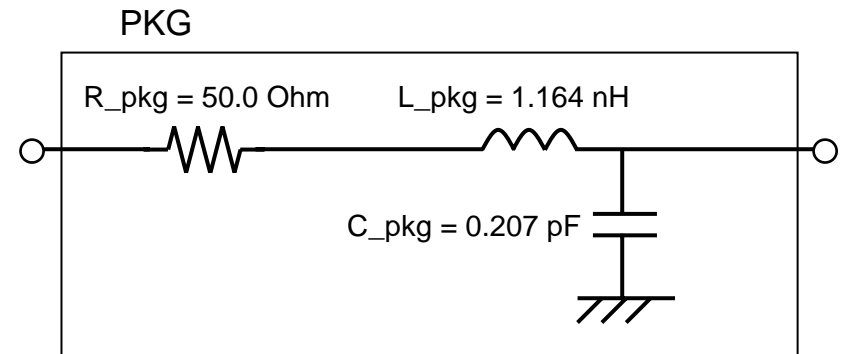
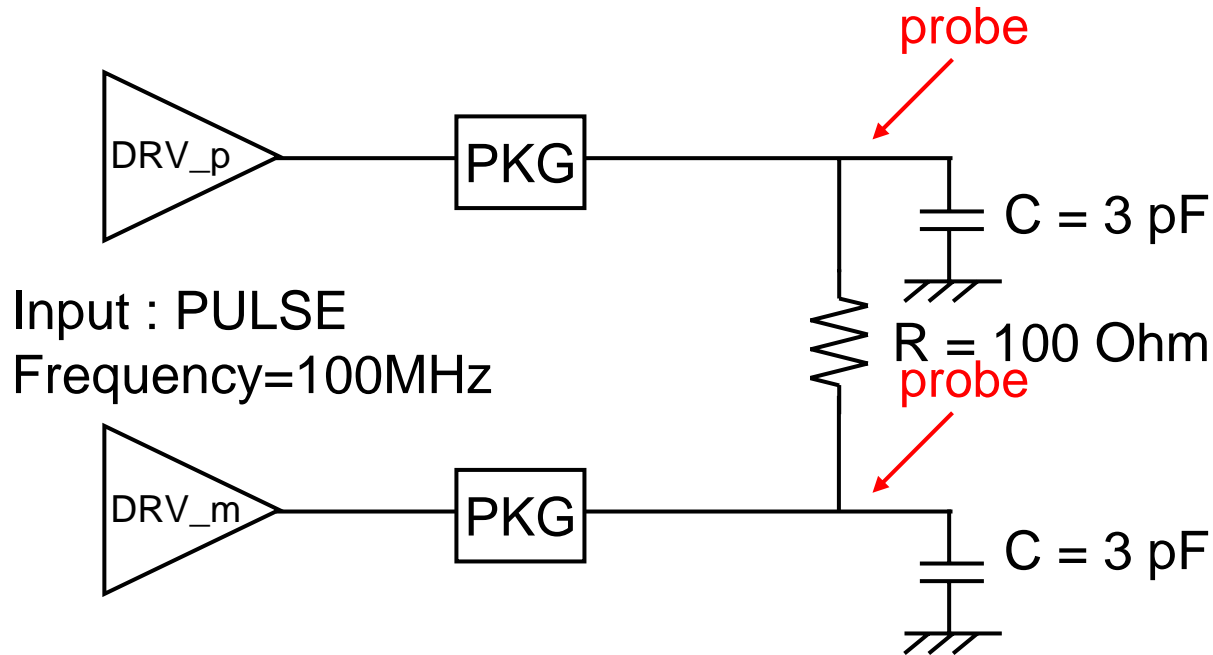
Differential Signal

Model type
3-state

Voltage range
3.3V

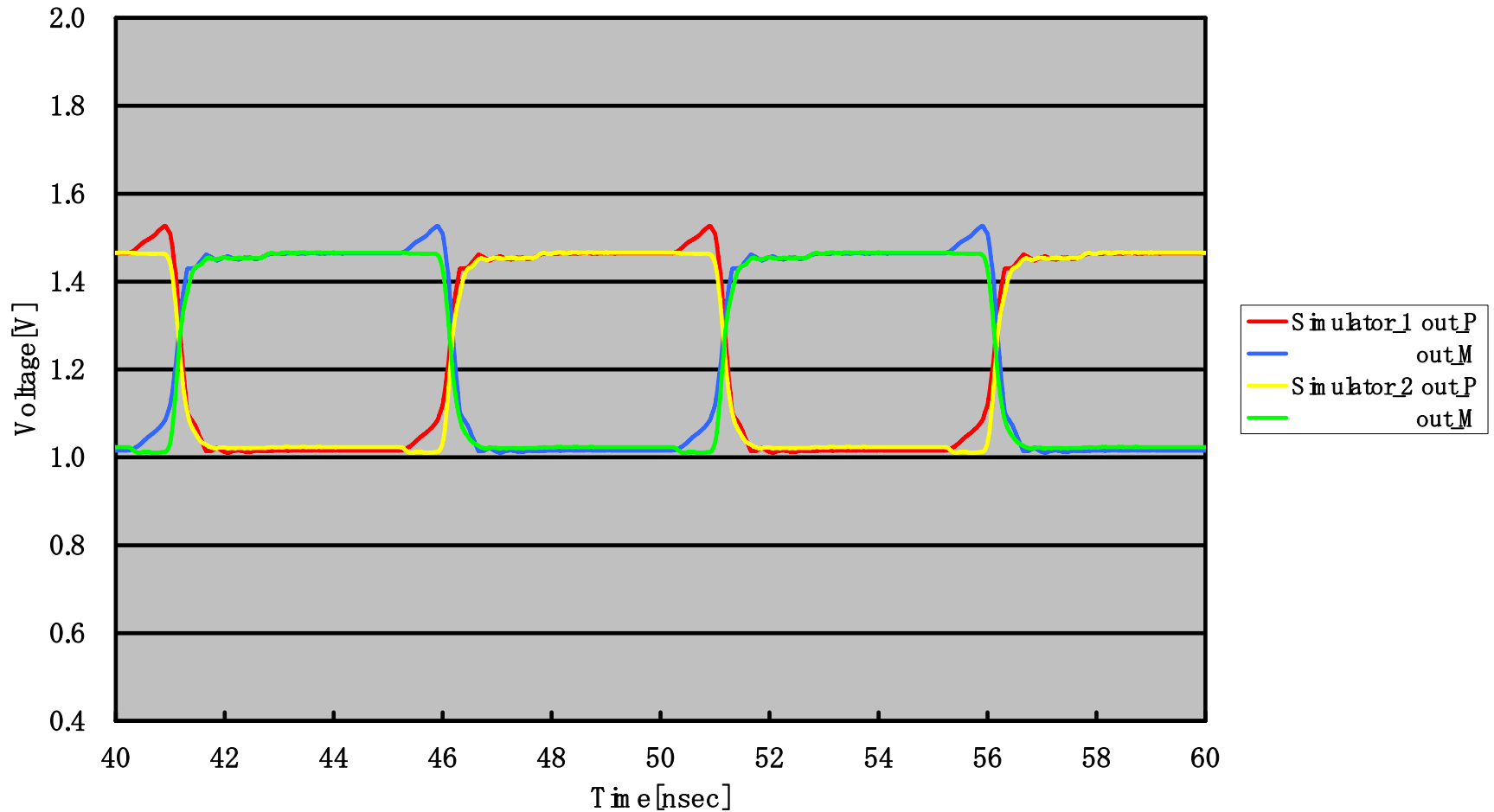
Used V-T data (ramp/waveform)
ramp

Evaluation circuit 3



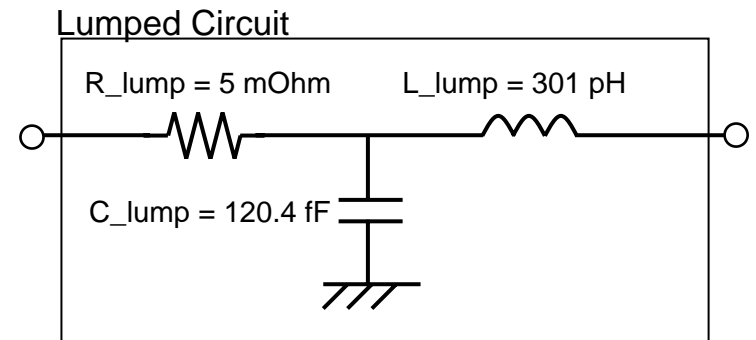
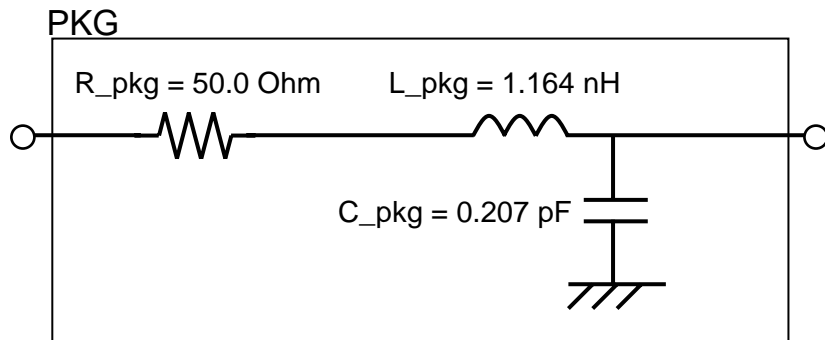
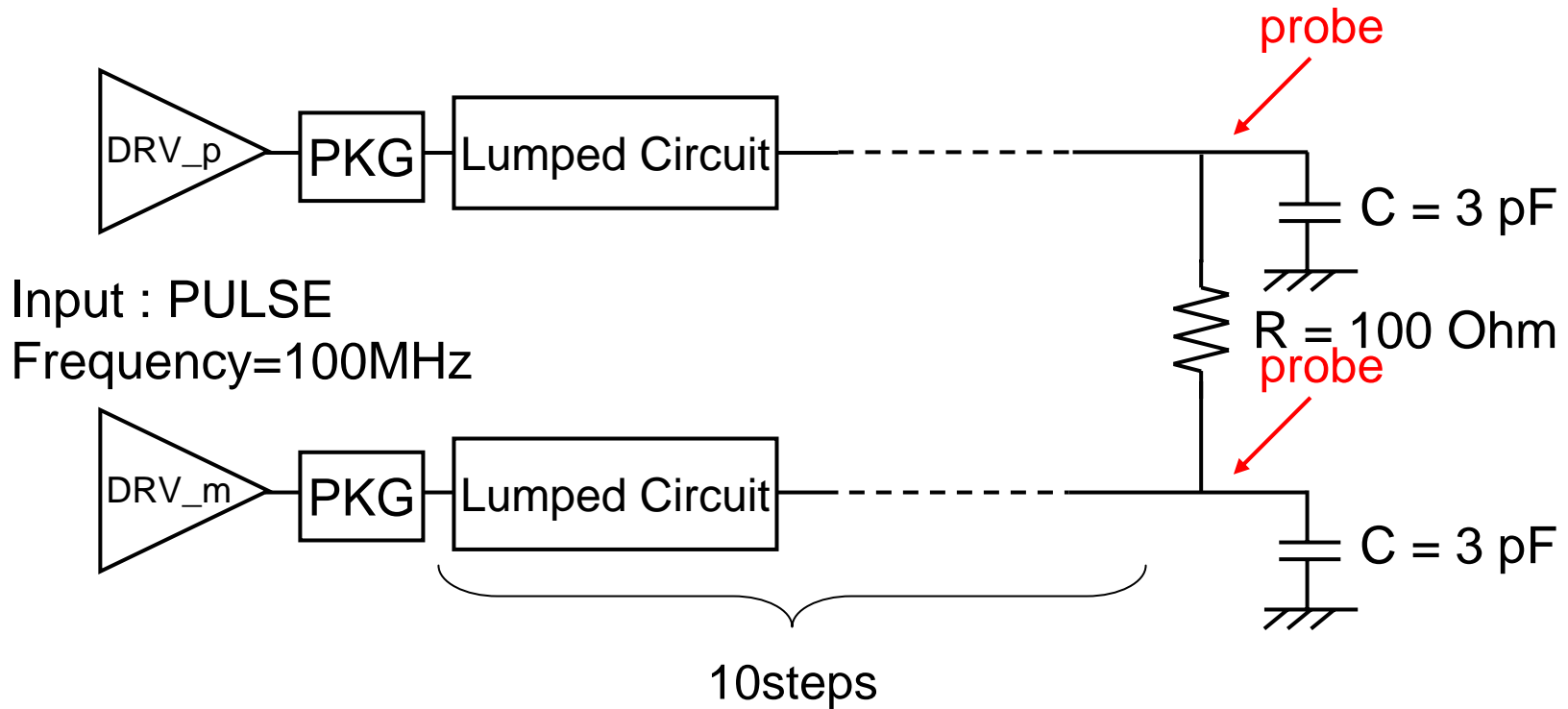
Result

Resistance+Capacitance termination



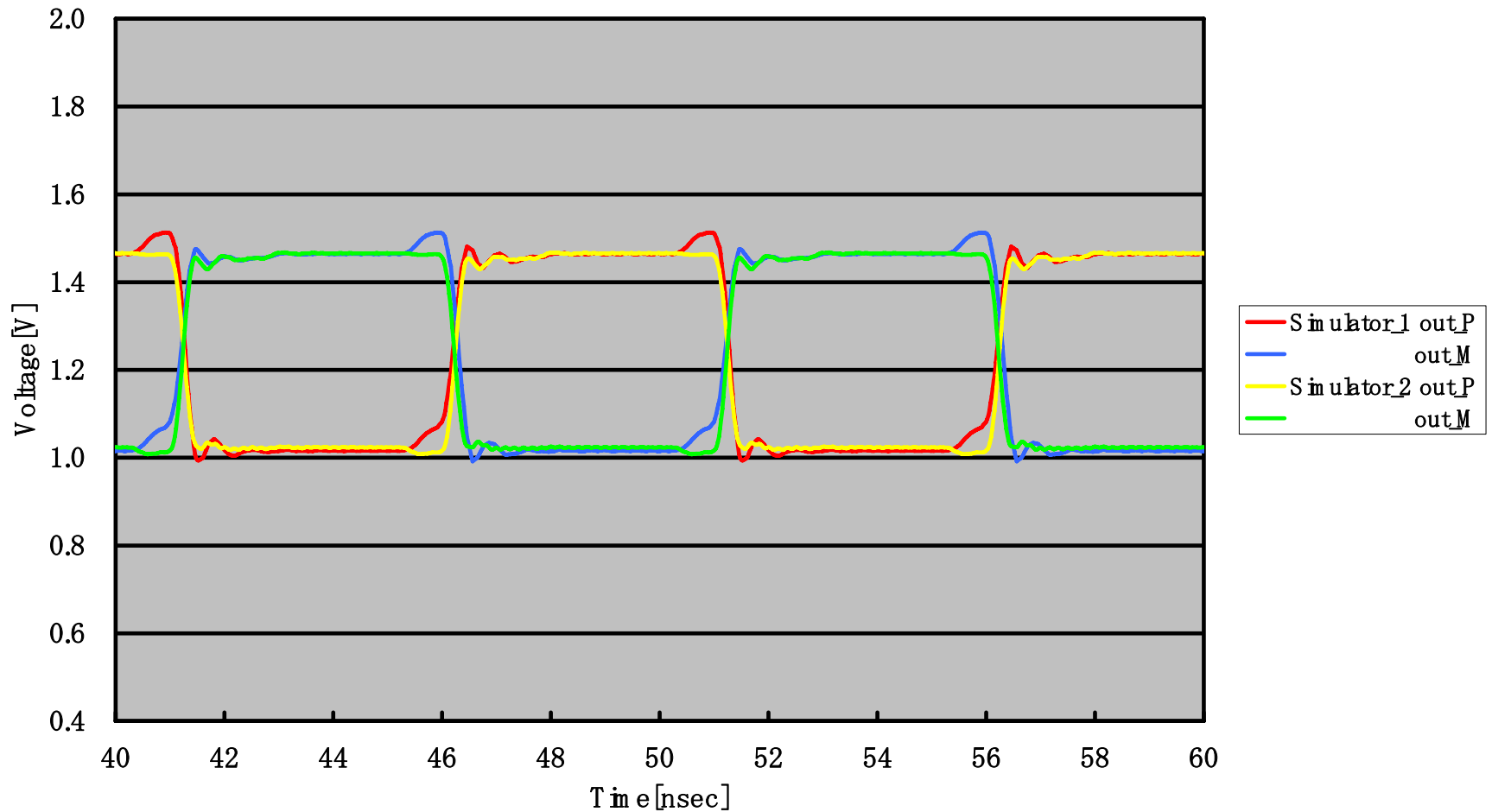
time adjustment

Evaluation circuit 4



Result

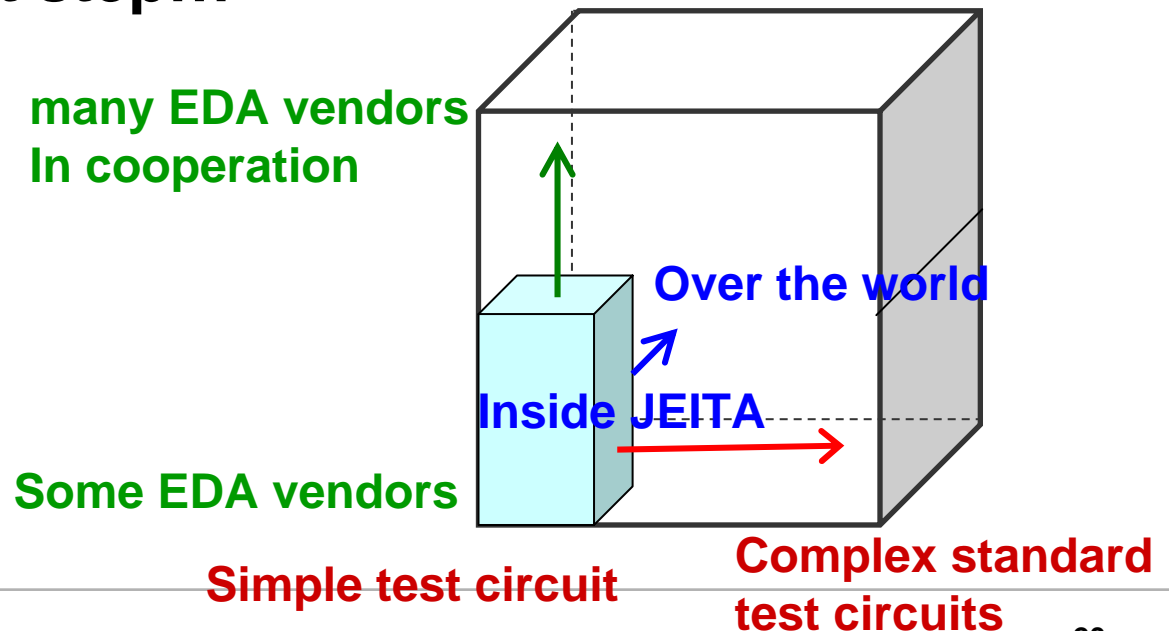
Transmission line (multistage lumped circuit)+Resistance+Capacitance termination



time adjustment

The next steps in this activity

1. **Considering test circuits for "IBIS Quality".**
Single / Differential model
simple 50Ohm resistance load
/ with complex transmission line
2. **Cooperating with the EDA vendors for this activity**
3. **Selecting IBIS Models from JEITA members**
4. **Planning the next step...**



In the future...

- **This activity is under preparation in present...**
- **JEITA hopes that many simulator vendors take part in our activity.**
- **We must expand and improve the standard test circuits.**
- **Finally, this test circuits will be public inside JEITA members. IBIS users (companies) will make use of test circuits for checking their simulation environments and proceeding operator's ability.**
- **If there is the same activity in EIA, let's join that.**
- **Verification and Validation are very important for ISO9001 in the near future.**

Thank you!!