



# The Case Study of Board Simulation

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(Panasonic)

# Panasonic digital appliance

## 🌟 Digital Appliance of Panasonic

panasonic.jp

 <p>ビューティ・タウ</p> <p>BS・110度CSデジタルハイビジョンテレビ</p>	 <p>ようこそ、プラズマリゾートへ。</p> <p>プラズマテレビ</p>	 <p>ハードディスクに録ってDVDに残す。</p> <p>Dream HS2 ハードディスク内蔵DVDビデオレコーダー</p>	 <p>空前画質!</p> <p>DIGICAM MX5000 液晶デジタルビデオカメラ</p>
 <p>Ayuは、こう聴く。</p> <p>!Dockin'style MD</p> <p>MJ55 ポータブルMDプレーヤー</p>	 <p>ライカの眼、加速。</p> <p>LUMIX デジタルカメラ</p>	 <p>こいつ、アセモノ</p> <p>D-snap</p> <p>AV30 SDマルチカメラ</p>	 <p>Ayuにハマりな。</p> <p>57 MD MDステレオシステム</p>
 <p>こんどの「P」は「カメラが2つ」</p> <p>ムーバP504iS 携帯電話</p>	 <p>「みんな」の行きたいところが「すぐに見つかる」</p> <p>YOUナビ HDDハードディスクナビ</p>	 <p>みんなのファクス、あたまが</p> <p>90CL パーソナル普通紙ファクス</p>	 <p>LIGHT LONG TOUGH</p> <p>Let's note LIGHT モバイルノートパソコン</p>

<http://panasonic.jp/>

# Agenda

- ☀ The Status of JEITA EDA-WG
- ☀ The Case Study of Board Simulation in Panasonic
- ☀ The Issues of Board Simulation
- ☀ Proposal to the IBIS-WG

# The Status of JEITA EDA-WG

## JEITA is developing "EDA Standard Dictionary"

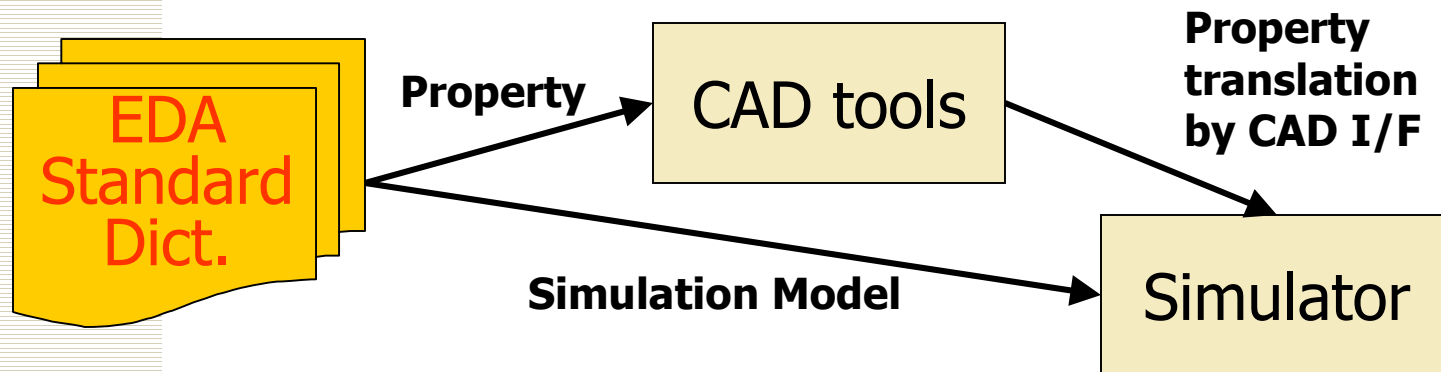
分類名称	CODE	ED	ERS	SI	CE	MS	IC	PREFNAME.EN	PREFNAME.JA	SHORTNAME.EN	SHORTNAME.JA
LQR/Q,Tr			001	Q				Model Select	解析情報有無	Model Select	解析情報有無
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Model description file	I,CLSI,SPICE モデル記述ファイル	Model file	モデル記述ファイル
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Circuit diagram	I,CLSI,SPICE 回路図	Circuit diagram	回路図
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Subcircuit node	I,CLSI,SPICE サブサーキットノード	Subcircuit node	サブサーキットノード
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Vt characteristics correlation	I,CLSI,SPICE Vt特性グラフ	Vt-character	Vt特性グラフ
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Tr/Tf characteristics correlation	I,CLSI,SPICE Tr/Tf特性グラフ	Tr/Tf-character	Tr/Tf特性グラフ
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Tr/Tf characteristics extraction code	I,CLSI,SPICE Tr/Tf特性抽出回路	Tr/Tf-extraction	Tr/Tf特性抽出回路
I,CLSI,SPICE			001	Q				I,CLSI,SPICE Simulator	I,CLSI,SPICE 解析ツール	Simulator	解析ツール
Tr,SPICE			001	Q				Tr,SPICE Model description file	Tr,SPICE モデル記述ファイル	Model file	モデル記述ファイル
Tr,SPICE			001	Q				Tr,SPICE Circuit diagram	Tr,SPICE 回路図	Circuit diagram	回路図
Tr,SPICE			001	Q				Tr,SPICE Subcircuit node	Tr,SPICE サブサーキットノード	Subcircuit node	サブサーキットノード
Tr,SPICE			001	Q				Tr,SPICE Vt characteristics correlation	Tr,SPICE Vt特性グラフ	Vt-character	Vt特性グラフ
Tr,SPICE			001	Q				Tr,SPICE Simulator	Tr,SPICE 解析ツール	Simulator	解析ツール
I,CLSI,IBIS			001	Q				I,CLSI,IBIS Version	I,CLSI,IBIS バージョン	Version	バージョン
I,CLSI,IBIS			001	Q				I,CLSI,IBIS Model description file	I,CLSI,IBIS モデル記述ファイル	Model file	モデル記述ファイル
I,CLSI,IBIS			001	Q				I,CLSI,IBIS Vt characteristics correlation	I,CLSI,IBIS Vt特性グラフ	Vt-character	Vt特性グラフ
I,CLSI,IBIS			001	Q				I,CLSI,IBIS Tr/Tf characteristics correlation	I,CLSI,IBIS Tr/Tf特性グラフ	Tr/Tf-character	Tr/Tf特性グラフ
I,CLSI,IBIS			001	Q				I,CLSI,IBIS Log file	I,CLSI,IBIS モデル記述チェックファイル	Log file	モデル記述チェックファイル
LDR,SPICE			001	Q				LDR,SPICE Model description file	LDR,SPICE モデル記述ファイル	Model file	モデル記述ファイル
LDR,SPICE			001	Q				LDR,SPICE Circuit diagram	LDR,SPICE 回路図	Circuit diagram	回路図
LDR,SPICE			001	Q				LDR,SPICE Subcircuit node	LDR,SPICE サブサーキットノード	Subcircuit node	サブサーキットノード
LDR,SPICE			001	Q				LDR,SPICE Frequency characteristics	LDR,SPICE 特性グラフ	F-character	特性グラフ
LDR,SPICE			001	Q				LDR,SPICE Simulator	LDR,SPICE 解析ツール	Simulator	解析ツール
LDR,S/パラメータ			001	Q				LDR,S Parameter Model description file	LDR,S/パラメータ モデル記述ファイル	Model file	モデル記述ファイル
LDR,S/パラメータ			001	Q				LDR,S Parameter Frequency range	LDR,S/パラメータ 周波数範囲	Frequency range	周波数範囲
LDR,S/パラメータ			001	Q				LDR,S Parameter Measurement condition	LDR,S/パラメータ 測定条件	Measurement	測定条件
LDR,S/パラメータ			001	Q				LDR,S Parameter Frequency characteristics	LDR,S/パラメータ 特性グラフ	F-character	特性グラフ
LDR,S/パラメータ			001	Q				LDR,S Parameter Simulator	LDR,S/パラメータ 解析ツール	Simulator	解析ツール

- Model circuit diagram, subcircuit node information, characteristics graph, verified simulator, ...

# The Status of JEITA EDA-WG

## ✦ Purpose of the "EDA Standard Dictionary"

- One category of ECALS dictionary(for EDI)
- Useful information for the components selection
- In order to perform simulation smoothly

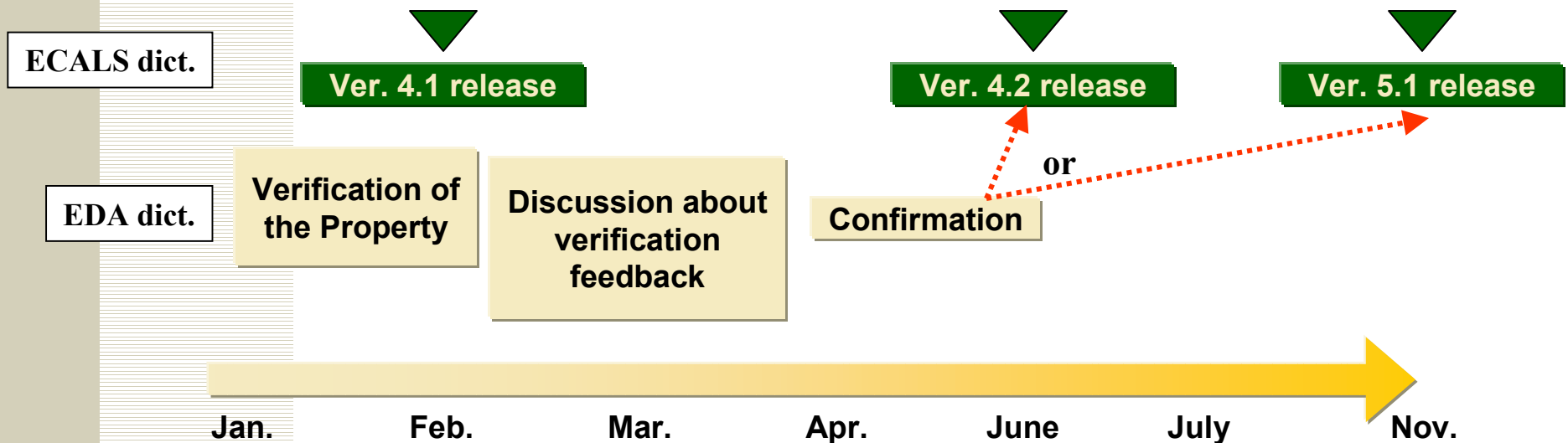


# The Status of JEITA EDA-WG

- ✦ "EDA Standard Dictionary" is in a verification stage
  - KYOCERA, Murata Manufacturing, TDK provided sample dictionaries
  - Appliance maker evaluated and verified those dictionaries
  - Feedback from appliance maker will be discussed at the EDA-WG

# The Status of JEITA EDA-WG

## ☀ "EDA Standard Dictionary" Development Schedule



Jan.27.2003

# Agenda

- ✦ The Status of JEITA EDA-WG
- ✦ **The Case Study of Board Simulation in Panasonic**
- ✦ The Issues of Board Simulation
- ✦ Proposal to the IBIS-WG

# The Case Study of Board Simulation

## ✦ Using Board Simulation for the Digital HDTV design

- Aim : Improvement of the picture quality
- Reduction of trial design
- Cost down



### – Approach:

- Direct connection of the digital picture stream data between the digital boards
  - Remove DAC/ADC from the board to board connection
- Placement and route optimization of the LSI and RAMs
  - Smaller area, reduction of the trial
- Improvement of the LSI

BSデジタル放送の美しさをそのまま再現。  
「デジタル直結処理回路」

BSデジタルチューナーからのデジタル信号を変換することなく映像処理し、広帯域化することで、BSデジタル放送の美しい高画質映像を鮮明に再現します。

([http://panasonic.jp/tv/products/hi\\_vision/feature/picture.html](http://panasonic.jp/tv/products/hi_vision/feature/picture.html))

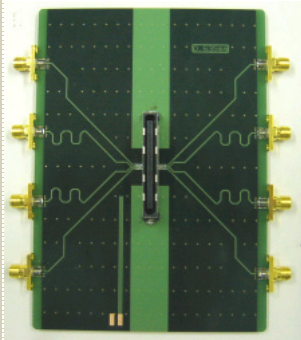
# The Case Study of Board Simulation

## Summary of the simulation(1)

- Direct connection of the digital picture stream data

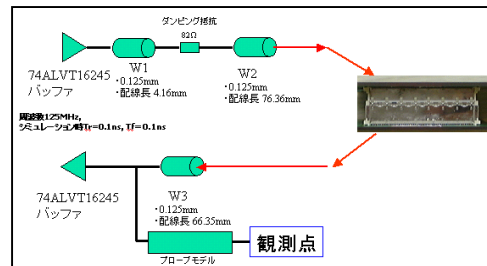
Next challenge

Extraction and Evaluation of the connector model



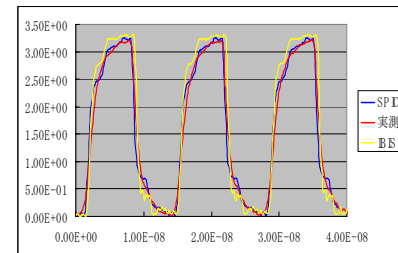
- Extraction of the SPICE model

Floor Plan simulation by SPICE, IBIS



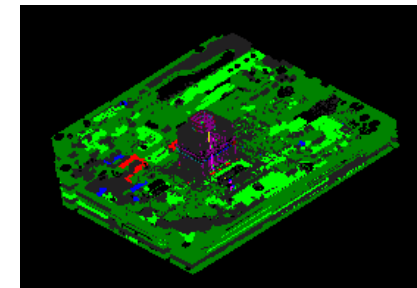
- Evaluation of the design condition (trace length, impedance, series resistor, ...)
- Crosstalk(connector pin assignment)

Evaluation of the simulation results



- Evaluation of the accuracy

Layout Simulation



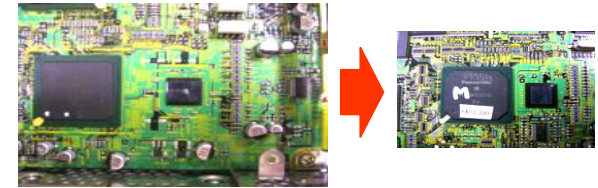
- Power/GND Analysis

# The Case Study of Board Simulation

## Summary of the simulation(2)

- Placement and route optimization of the LSI and RAMs

- Optimization of the trace impedance
- Examination of the driver abilities
- Termination
- Crosstalk
- Signal Integrity



- 4 layers Rambus
- 6 layers smaller area (Achieve 60%)



Expansion of the Rambus rules  
and make Panasonic rules

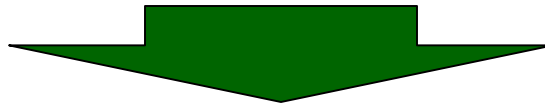
# Agenda

- ✦ The Status of JEITA EDA-WG
- ✦ The Case Study of Board Simulation in Panasonic
- ✦ **The Issues of Board Simulation**
- ✦ Proposal to the IBIS-WG

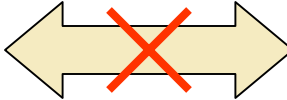
# The Issues of Board Simulation

## ✦ Background and issues

- Transient analysis is useful for the digital appliance
  - SI simulator or SPICE is useful
- S-parameter model is often supplied for High frequency(RF) components



Higher frequency digital = Using RF components

Time domain  Frequency domain

**Freq. Domain model is not useful!**

# The Issues of Board Simulation

## Approaches ... 2 types of approaches

### – Using RF simulator

○ • S-parameter model can be used directly

△ • Time domain module is often option(i.e. more cost)

✗ • IBIS, SPICE models cannot be used for ICs

○ : OK  
△ : So so  
✗ : NG

### – Translation S-parameter model to SPICE model

○ • Simulator can be used as it is(i.e. no more cost)

? • Translation accuracy → Evaluation this time!

# The Issues of Board Simulation

## 🔧 Description of the translation

- Translation S-parameter to SPICE model
  - Using BroadBand Spice (Sigrity)

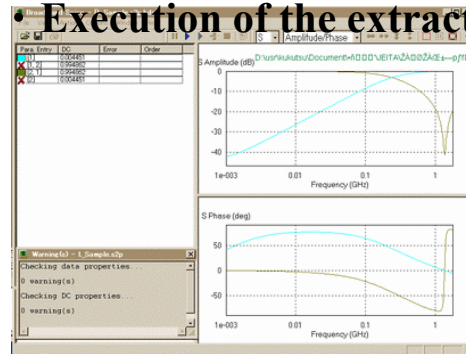
**Read and check  
S-parameter**

- Format checking
- Calculate DC value

**Extraction**

- Choose types of export model

### • Execution of the extraction

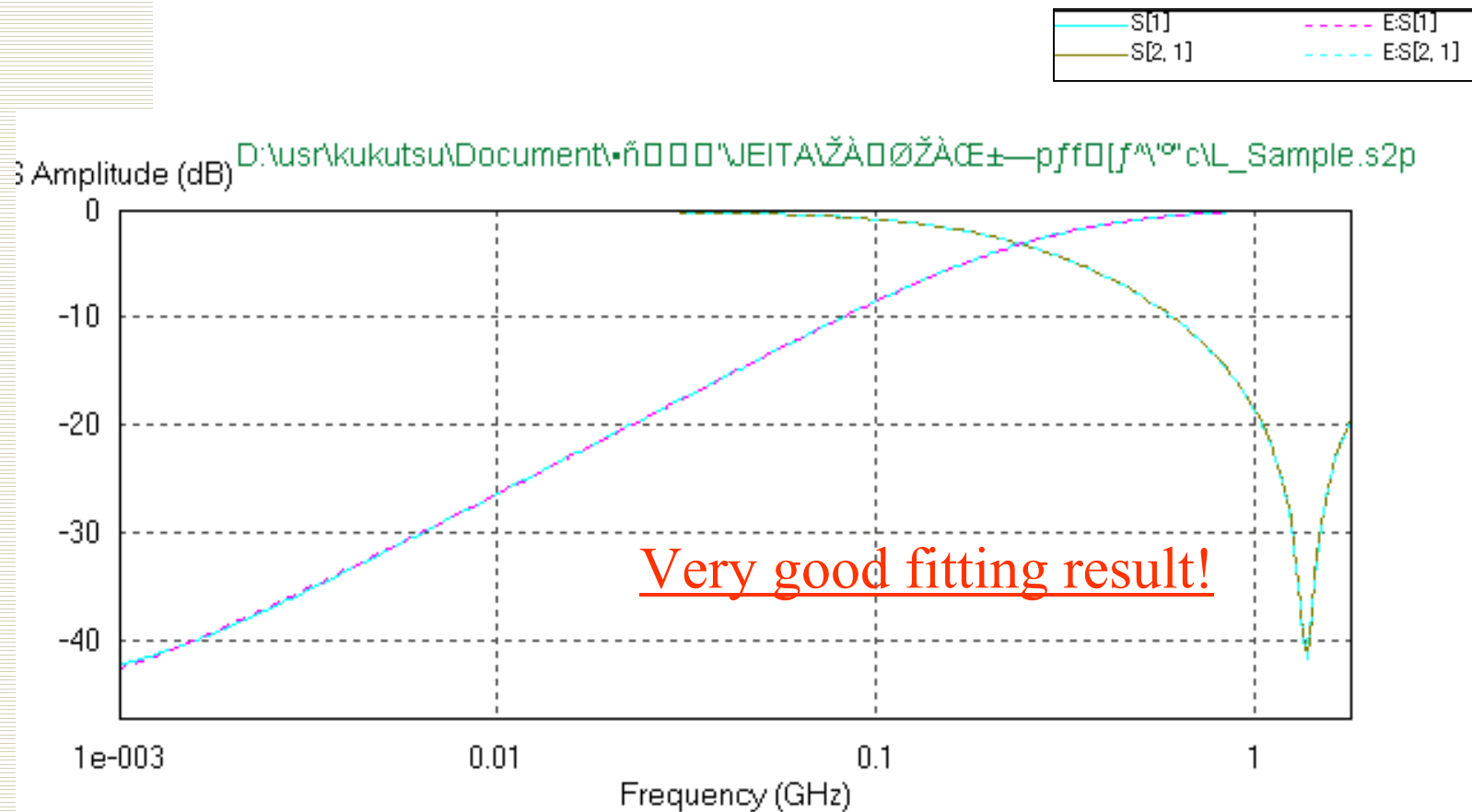


**Result Check**

- Check waveforms
- Re-fitting if necessary

# The Issues of Board Simulation

## ✦ Extraction result (1)





# The Issues of Board Simulation

## ✂ Extraction result ... Extracted models

### HSPICE native format

```
* This is the subcircuit netlist generated by Broadband
SPICE v1.0
* Port Number: 2.
* HSPICE compatible
.subckt L_Sample 1 2 ref
Rd1_1      3 ref 50
Rd1_2      4 ref 1
Vd1        1 3 0
F1         ref 4 Vd1 1.0
G1         ref 4 1 ref      0.02
Rd2_1      5 ref 50
Rd2_2      6 ref 1
Vd2        2 5 0
F2         ref 6 Vd2 1.0
G2         ref 6 2 ref      0.02

G3 ref 3 LAPLACE 4 ref
+ -4.2194949336101296e+016
+ -7.6924500349367864e+005
+ /
+ 8.0538254790796067e+019
+ 1.1053698816035342e+009
+ 1
```


### General SPICE format

```
* This is the subcircuit netlist generated by Broadband
SPICE v1.0
* Port Number: 2.
* SPICE compatible
.subckt L_Sample 1 2 ref
Rd1_1      3 ref 50
Rd1_2      4 ref 1
.
.
.
L2_3_0 n1_1_2 n1_1_par0 2.6196734419533908e-008
C2_3_0 n1_1_par0 n1_1_0 4.7396975379644448e-013
R2_3_0 n1_1_par0 n1_1_0 1.9087178929704005e+003
L1_3_0 p1_1_2 p1_1_ser0 2.6735500391528574e-008
C1_3_0 p1_1_ser0 p1_1_serd0 4.6441845416260152e-013
R1_3_0 p1_1_serd0 p1_1_0 2.9552616902395183e+001

L2_3_1 n1_1_2 n1_1_par1 2.4621677645809129e-007
C2_3_1 n1_1_par1 n1_1_0 6.6348538919814883e-014
R2_3_1 n1_1_par1 n1_1_0 4.8138425989128831e+004
L1_3_1 p1_1_2 p1_1_ser1 2.2790661272104553e-007
C1_3_1 p1_1_ser1 p1_1_serd1 7.1679023177516205e-014
R1_3_1 p1_1_serd1 p1_1_0 7.1356522526650309e+001
```

# The Issues of Board Simulation

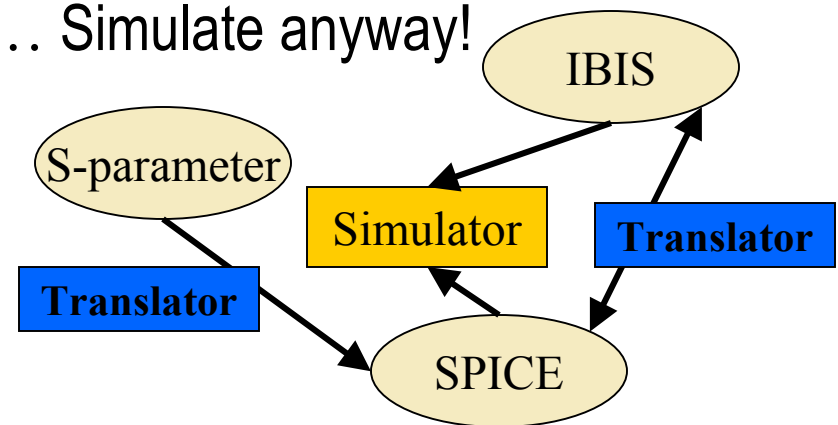
## Wrap up

- S-parameter model can be applied for time domain simulation  Expansion of the simulation case
- Examination of the accuracy would be necessary
  - S-parameter extracted conditions(frequency range, ...)
  - Theoretical limitation
  - Characteristics of the components

# The Case Study of Board Simulation

## Next Step

- Expansion of the Model Extraction Environment
  - Although semiconductor component would be difficult, we would like to increase more types of passive components
- Construction of the simulation environment which can handle various model format
  - 1st step: Model translation ... Simulate anyway!
  - 2nd step: More accuracy



# Agenda

- ✦ The Status of JEITA EDA-WG
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- ✦ The Issues of Board Simulation
- ✦ **Proposal to the IBIS-WG**

# Proposal to the IBIS-WG

## Requirement to the models(more accuracy)

- More useful 'variation' parameters
  - Min/Max is not for useful because those conditions are not likely on the board.
  - Practical 'variation' conditions, range(number of condition, e.g. typ1, typ2, or ,10degree, 25degree, 40degree, 80degree, ...) would be necessary
  - 'variation' parameter of each production lot would be useful

# Proposal to the IBIS-WG

- ✦ Co-operation between IBIS-WG and JEITA EDA-WG to improve board simulation environment
  - IBIS-WG: LSI, Package, module model accuracy
  - JEITA EDA-WG: Feedback board simulation study result

