I/O Buffer Accuracy Report

Part Number	74ALVCH16831DF
Package	80-pin TVSOP
Manufacturer	IDT

Revision 2.1
September 11, 2000

Revision History

1.0 April 20, 2000
Greg Edlund, IBM

2.0 August 22, 2000
Greg Edlund, IBM
Built a new batch of test boards with new sample parts from the same lot. Repeated all measurements using same components at IBM and IDT. Measured capacitance using HP54740 TDR; results were much improved. Measured IV curves using DVM and power supply to expand current limit beyond 100 mA. Reran HSPICE simulations using coupled package model and lossy transmission line model. Regenerated IBIS model datasheet using capacitance numbers from HSPICE simulations and IDT package modeling group.

2.1 September 11, 2000
Greg Edlund, IBM
Added IBIS data to section 4. Corrected various typos found by IDT.

Several people contributed to this report. Ryan Schlichting designed the test board. Wes Martin and Mike McCormack took the waveforms and capacitance data. Scott Seim measured the junction temperature. Pat Zabinski took the IV curves. Matt Callicoat generated the IBIS datasheet, ran simulations, and did the data analysis. Greg Edlund wrote the report. Toby Schaffer and Roland Knaack provided engineering support from IDT. Thanks to all.

Table of Contents

1. Test Conditions

1.1 Semiconductor Processing

The component we tested was a random sample from lot ED00746G (Korea JP). IDT reported that this lot showed parametric data consistent with +/- 1σ process, and the lab data corroborate this.

1.2 Test Environment

We set VDD = 3.3 V at the DUT in all of our lab measurements. Using θjc, power, and a thermal image of the DUT, we calculated the junction temperature to be 36C.

Table 1: Test Board Electrical Parameters

Parameter	Description	Value	Units
Cpad	Pad capacitance	0.4	pF
Cprobe	Probe capacitance	0.8	pF
Tpd	Propagation delay	185	ps/in.
Zo	Characteristic impedance	54	Ω

1.3 Test Equipment

Table 2: Test Equipment

Model	Description	Serial No.	Cal Due
HP 54720	Digital oscilloscope	3249A00346	9-11-99
HP 54721A	Amplifier	3246A00131	9-11-99
HP 54750A	Digital oscilloscope	N/A	N/A
HP 54754A	Differential TDR module	N/A	N/A
HP 4275A	LCR meter	N/A	N/A
Tek DMM912	Digital multimeter	N/A	N/A
HP 8116A	Signal generator	3001A07967	9-21-00
HP E3632A	Power supply	KR75305682	7-8-00

We used an integrated 1K probe with a 0.100 in. square post header as described by Howard Johnson in "High Speed Digital Design." The bandwidth of the HP 54721A amplifier is 1.1 GHz. It samples at 4 Gsa/s, and we acquired data in average mode with N = 32. The rise time of the HP 75454A TDR is 30 ps.

2. Lab vs. SPICE Correlation

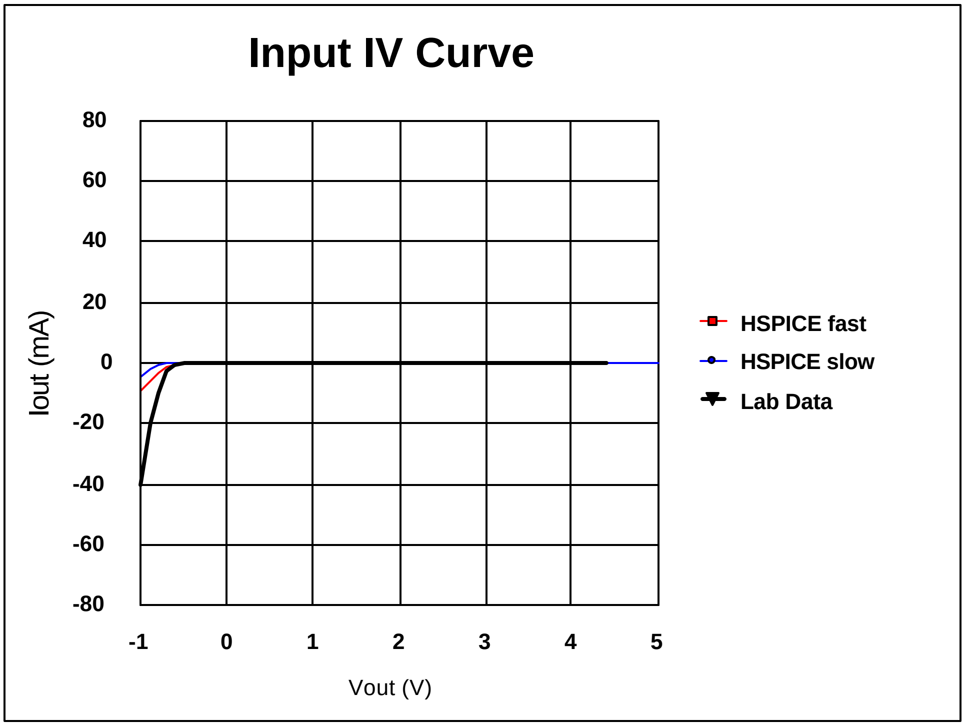
2.1 Component Electrical Parameters

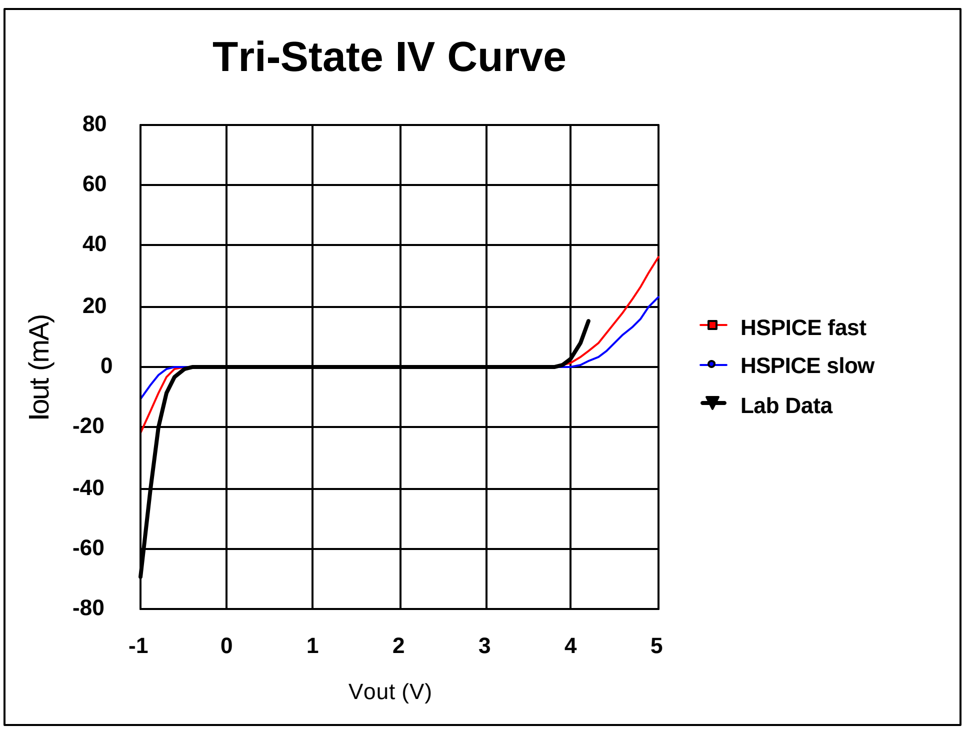
Table 3: Component Electrical Parameters

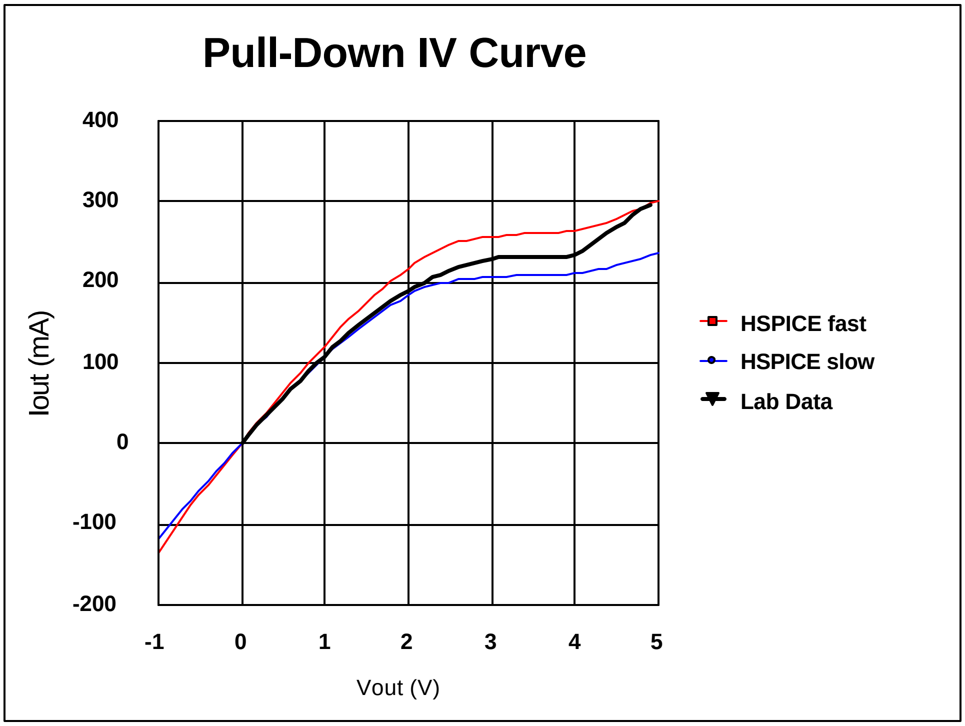
Parameter	SPICE Min	SPICE Typ	DUT	SPICE Max	Units
Cin	2.3	2.9	2.6	3.8	pF
Cout	5.5	7.4	6.5	9.3	pF
Dvdtr	3.6	4.1	5.5	4.5	V/ns
Dvdtf	6.0	6.9	8.2	7.8	V/ns
Zoutr	13	14	14	16	Ω
Zoutf	8.3	8.8	8.0	9.3	Ω

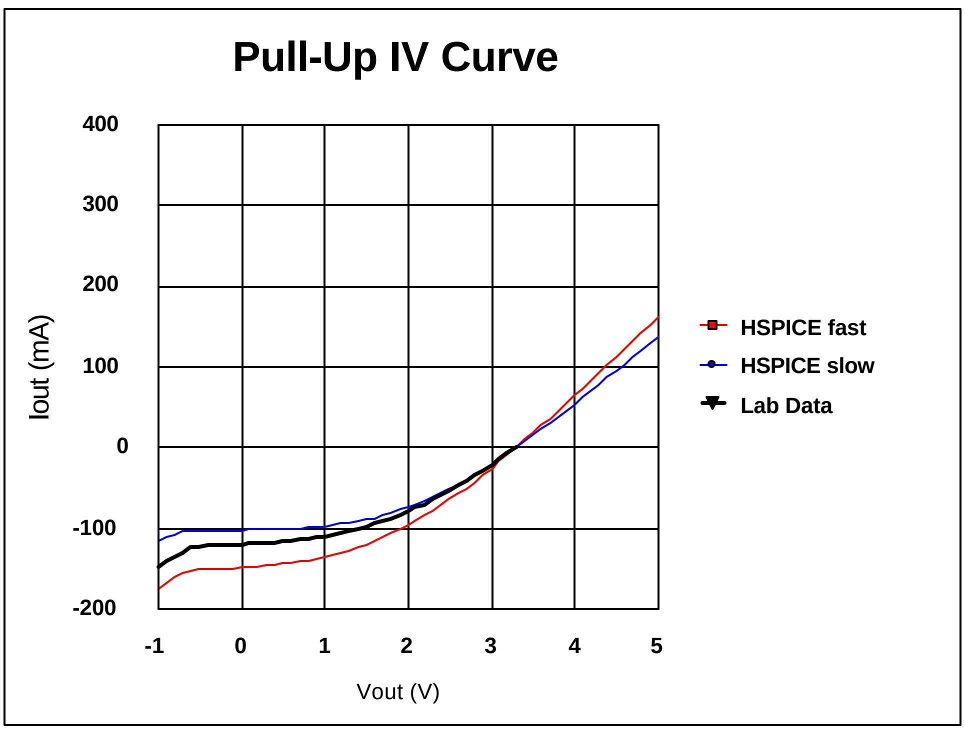
We used VDD = 3.3 V and Tj = 36C (lab conditions) in all of our HSPICE analysis in section 2 of this report. To generate the above chart, we varied process conditions but not voltage or temperature. We used the 50 Ω loads to extract the edge rates and output impedances. In order to achieve a high degree of correlation, we had to use coupled package models (corner and side sections) and a lossy transmission line model, i.e. HSPICE w-element.

2.2 IV Curves

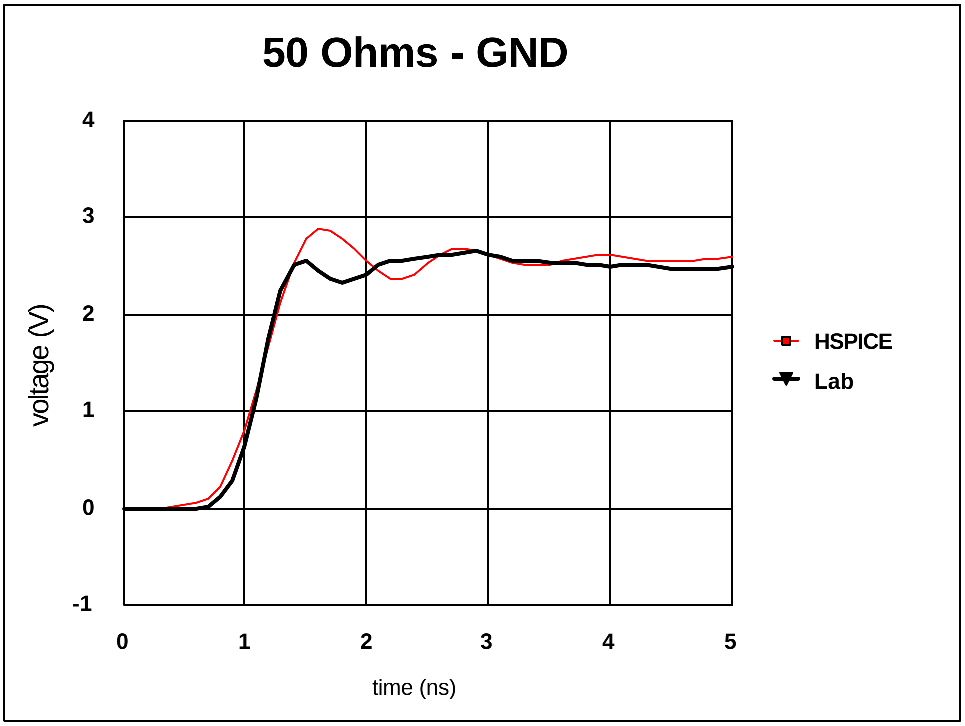

Input IV Curve
80
60
40
20
0
-20
-40
-60
-80
Iout (mA)
-1
0
1
2
3
4
5
Vout (V)
HSPICE fast
HSPICE slow
Lab Data

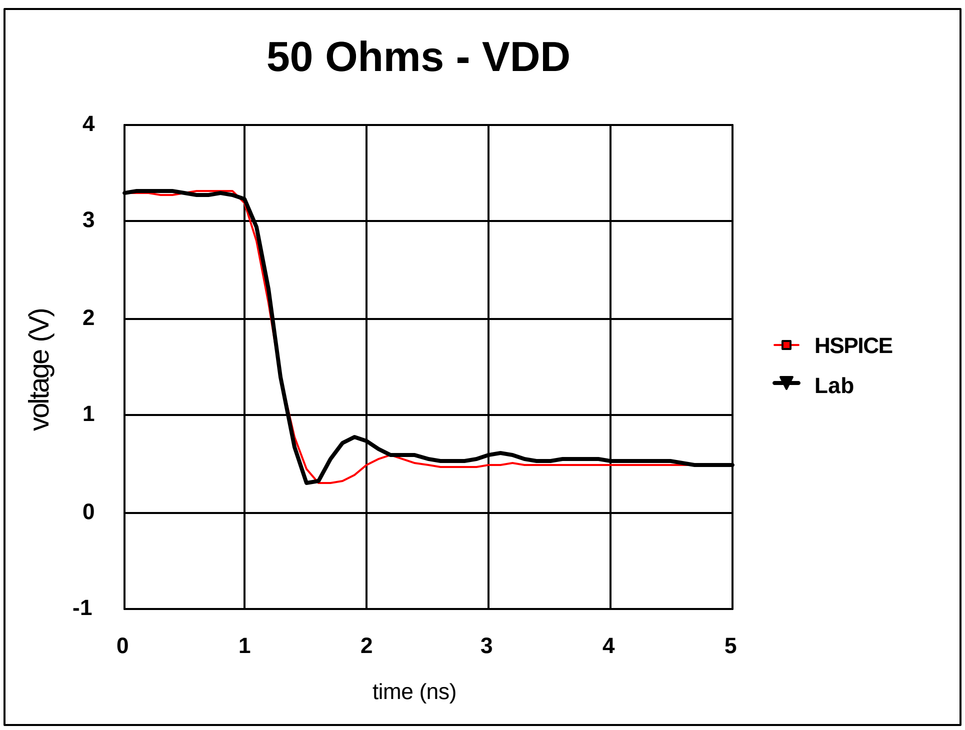

Tri-State IV Curve
80
60
40
20
0
-20
-40
-60
-80
Iout (mA)
-1
0
1
2
3
4
5
Vout (V)
HSPICE fast
HSPICE slow
Lab Data

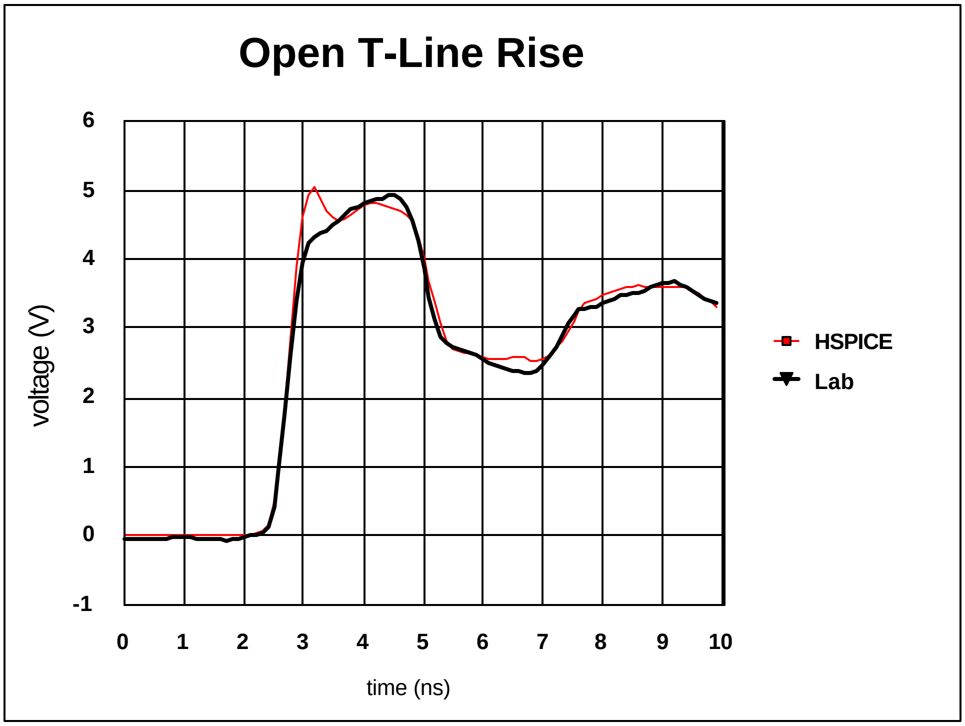

Pull-Down IV Curve
400
300
200
100
0
-100
-200
Iout (mA)
-1
0
1
2
3
4
5
Vout (V)
HSPICE fast
HSPICE slow
Lab Data

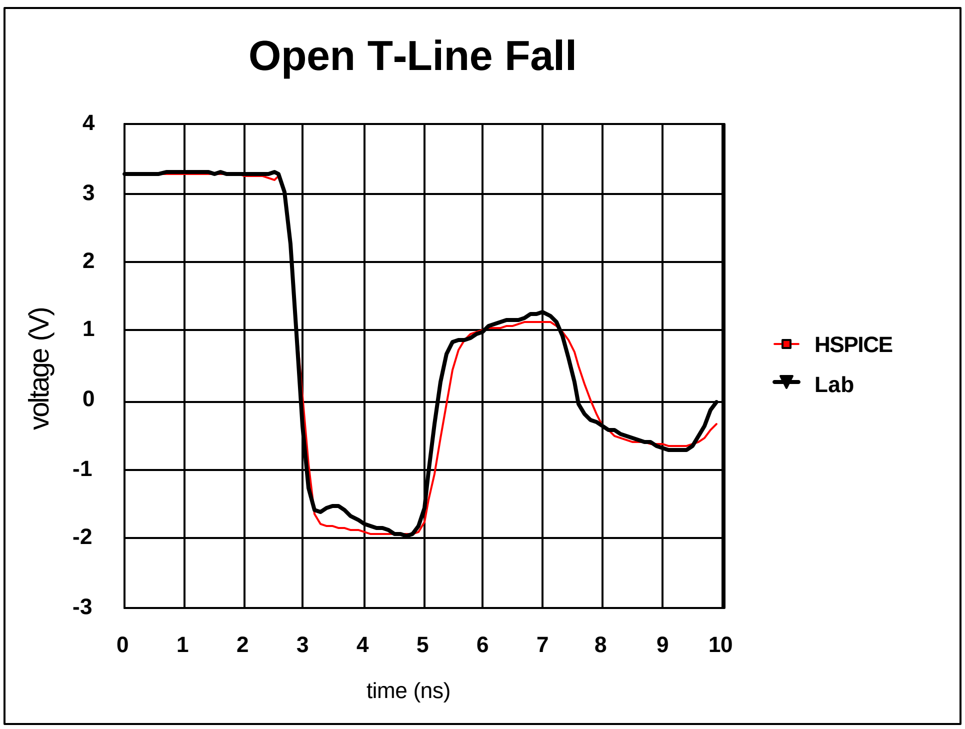

Pull-Up IV Curve
400
300
200
100
0
-100
-200
Iout (mA)
-1
0
1
2
3
4
5
Vout (V)
HSPICE fast
HSPICE slow
Lab Data

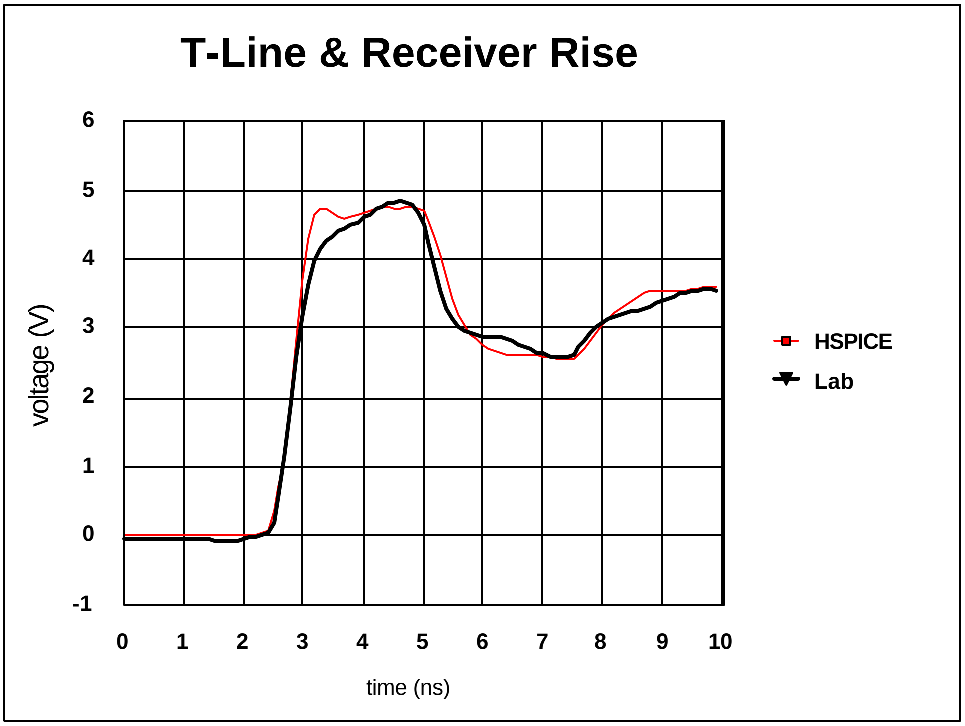
2.3 Test Load Waveforms

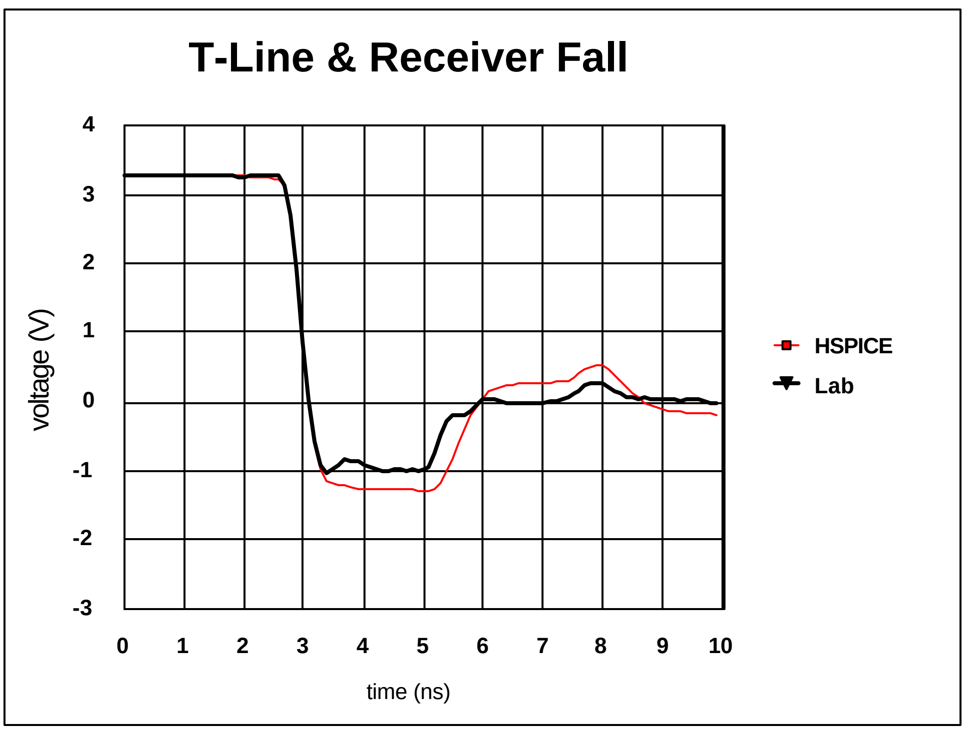


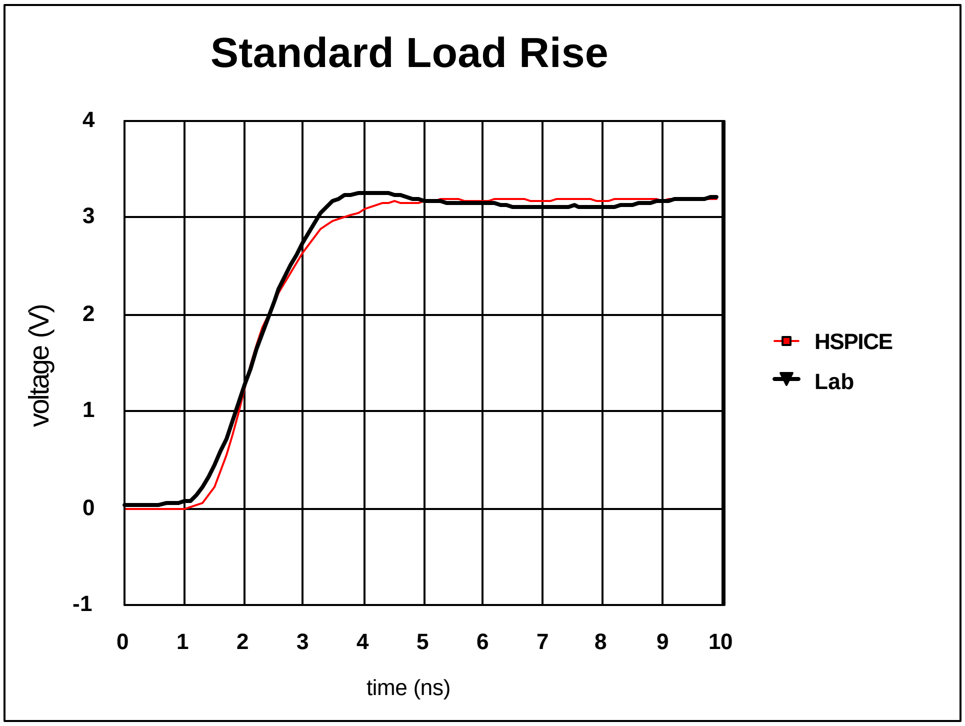


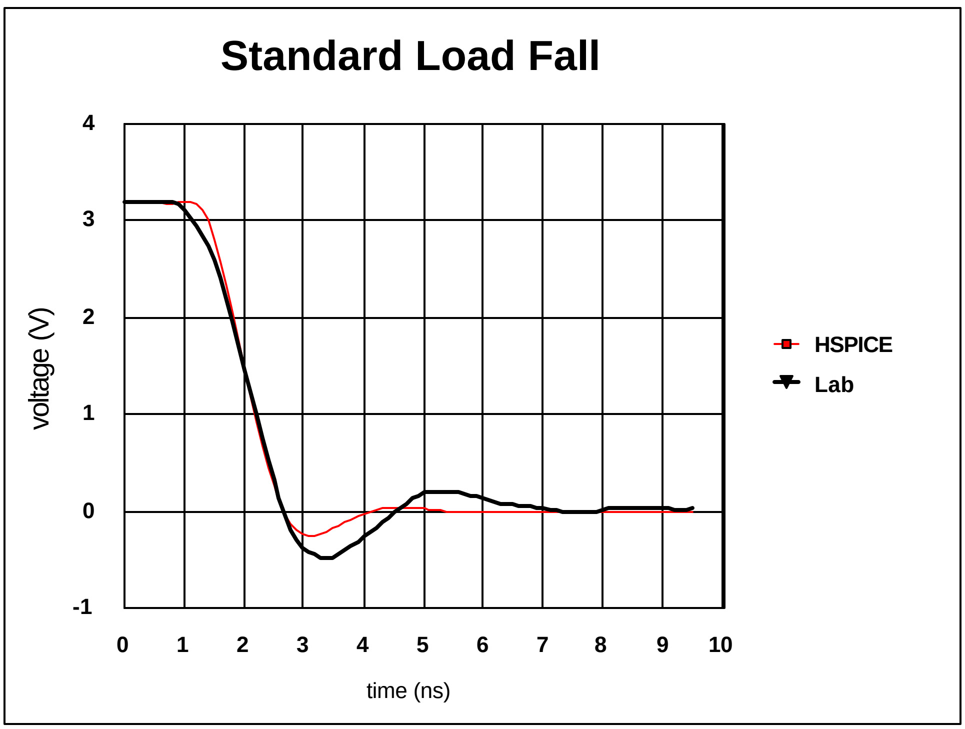

Open T-Line Rise
voltage (V)
6
5
4
3
2
1
0
-1
0
1
2
3
4
5
6
7
8
9
10
time (ns)
HSPICE
Lab


Open T-Line Fall
voltage (V)
4
3
2
1
0
-1
-2
-3
0
1
2
3
4
5
6
7
8
9
10
time (ns)
HSPICE
Lab


T-Line & Receiver Rise
voltage (V)
6
5
4
3
2
1
0
-1
0
1
2
3
4
5
6
7
8
9
10
time (ns)
HSPICE
Lab


T-Line & Receiver Fall
voltage (V)
4
3
2
1
0
-1
-2
-3
0
1
2
3
4
5
6
7
8
9
10
time (ns)
HSPICE
Lab


Standard Load Rise
voltage (V)
4
3
2
1
0
-1
0
1
2
3
4
5
6
7
8
9
10
time (ns)
HSPICE
Lab


Standard Load Fall
voltage (V)
4
3
2
1
0
-1
0
1
2
3
4
5
6
7
8
9
10
time (ns)
HSPICE
Lab

2.4 Figures of Merit

Table 4: Lab vs. HSPICE Figures of Merit

Measurement	Envelope	Overlay
Input IV curve	Fail	
Output tri-state IV curve	Fail	
Output pull-down IV curve	Pass	
Output pull-up IV curve	Pass	
50 Ω to GND		97.04%
50 Ω to VDD		98.18%
Open T-line rising		96.97%
Open T-line falling		96.29%
T-Line and receiver rising		96.16%
T-Line and receiver falling		94.92%
Standard load rising		97.85%
Standard load falling		97.09%

These figures of merit are based on the correlation metrics defined in the “I/O Buffer Accuracy Handbook.”

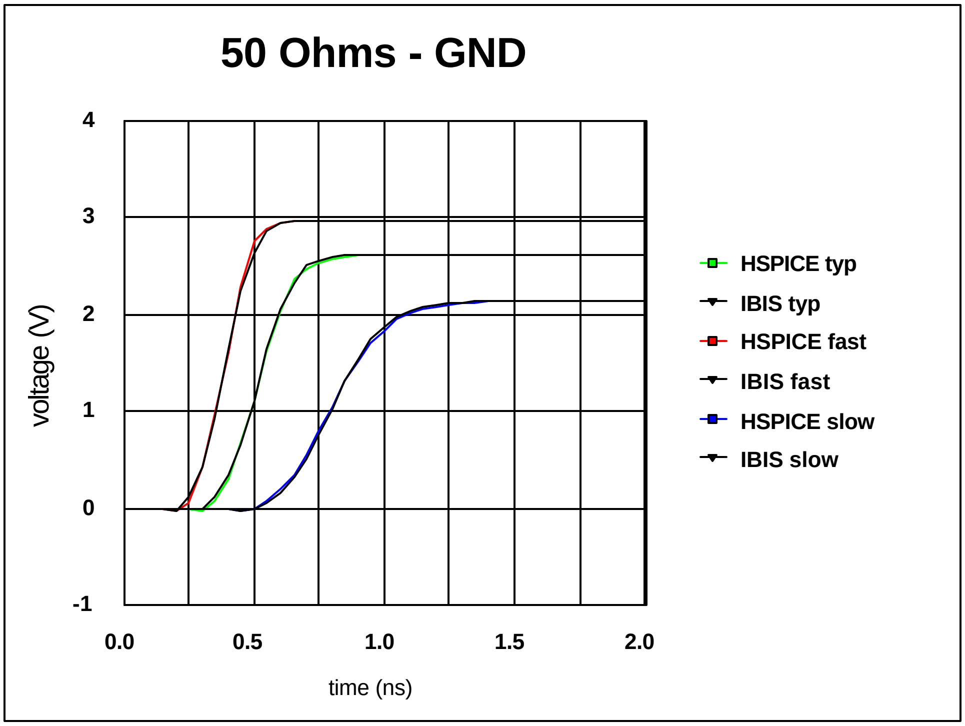
2.5 Discrepancies

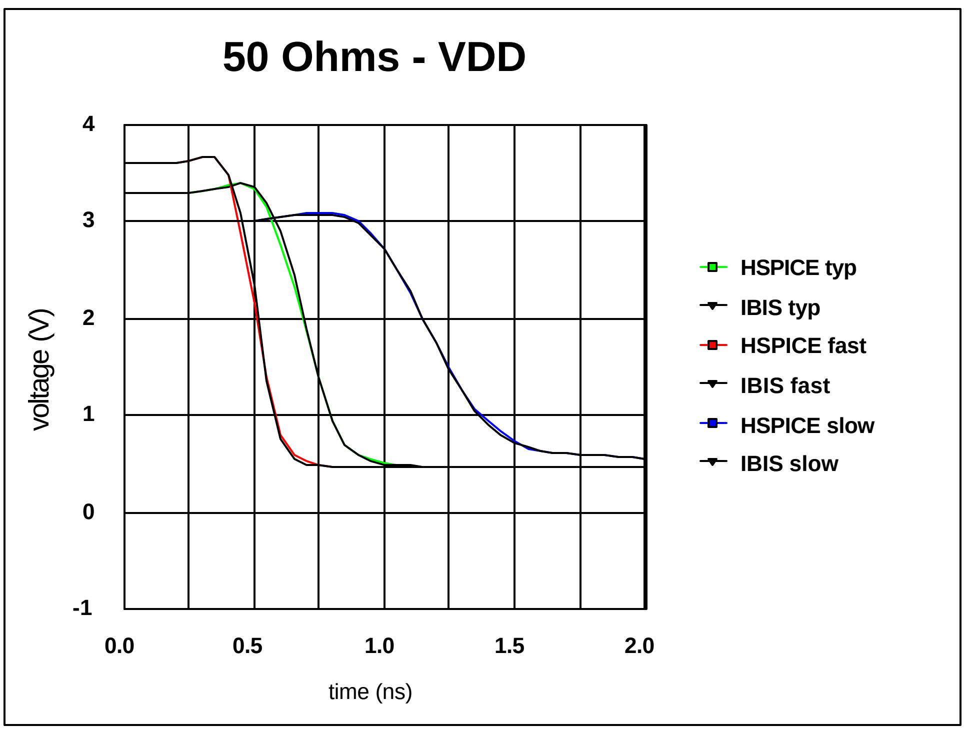
The input and tri-state IV curves show that the actual ESD diodes are stronger than those in the HSPICE model. This discrepancy also shows up in the transmission line and receiver load where the DUT clamps at a higher voltage than the HSPICE simulations predict.

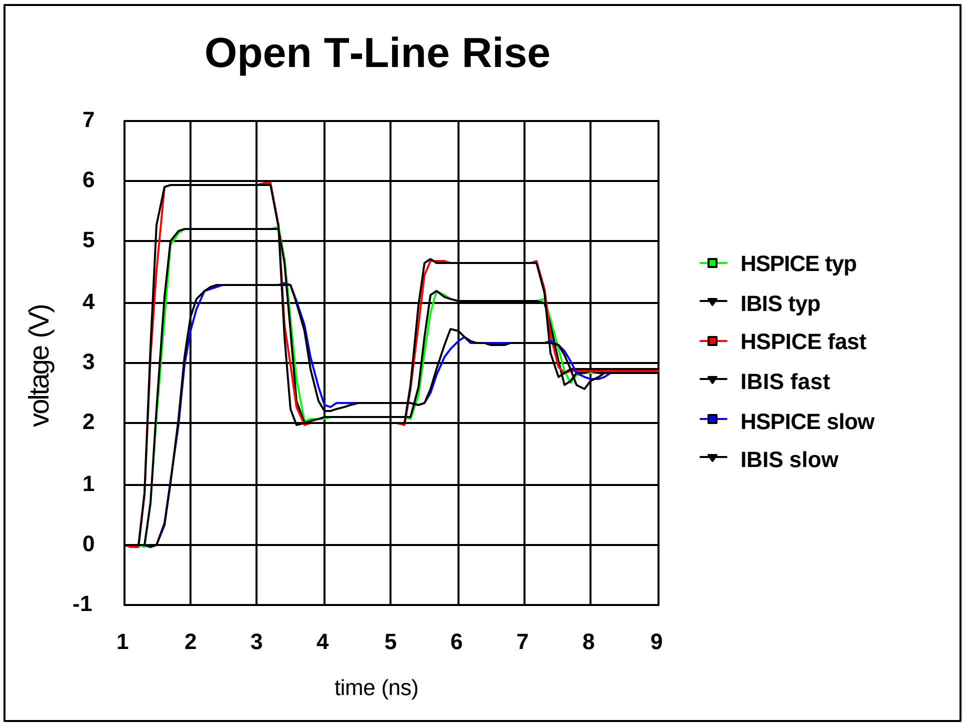
The two 50 Ω loads demonstrate a lower amplitude and higher frequency ringing in the lab. I suspect that the coupled package model or the power distribution model needs some refinement.

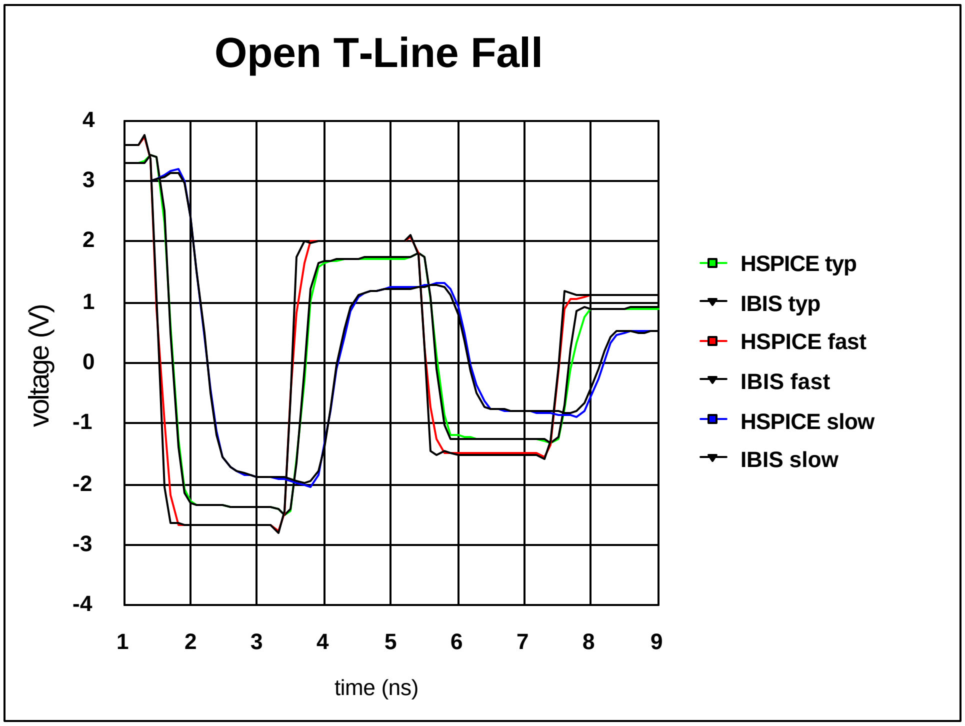
3. IBIS vs. HSPICE Correlation

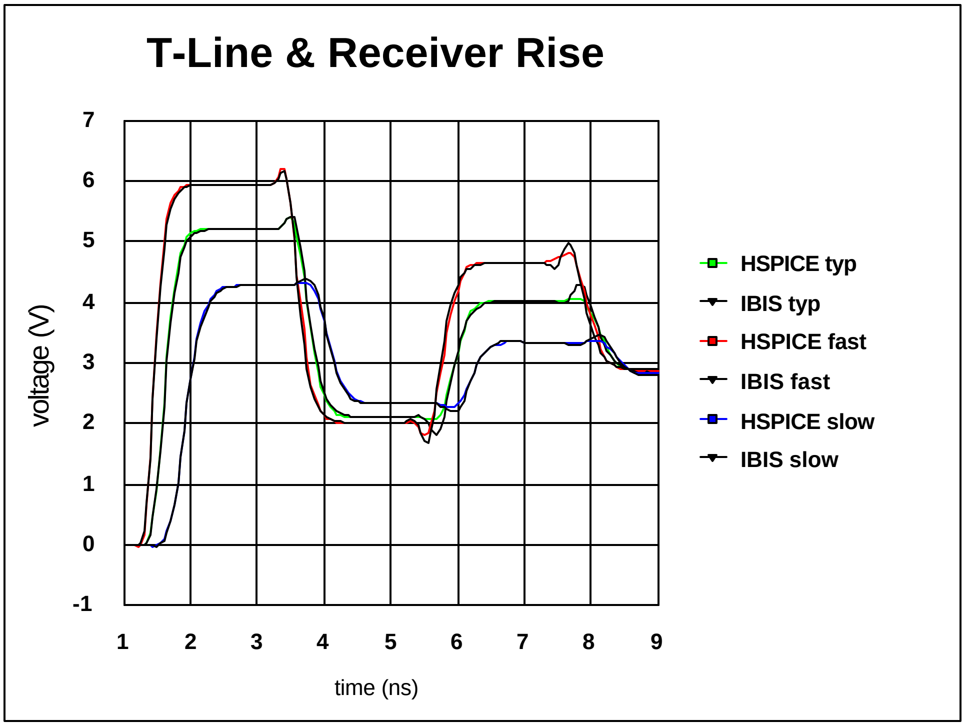
3.1 Test Load Waveforms

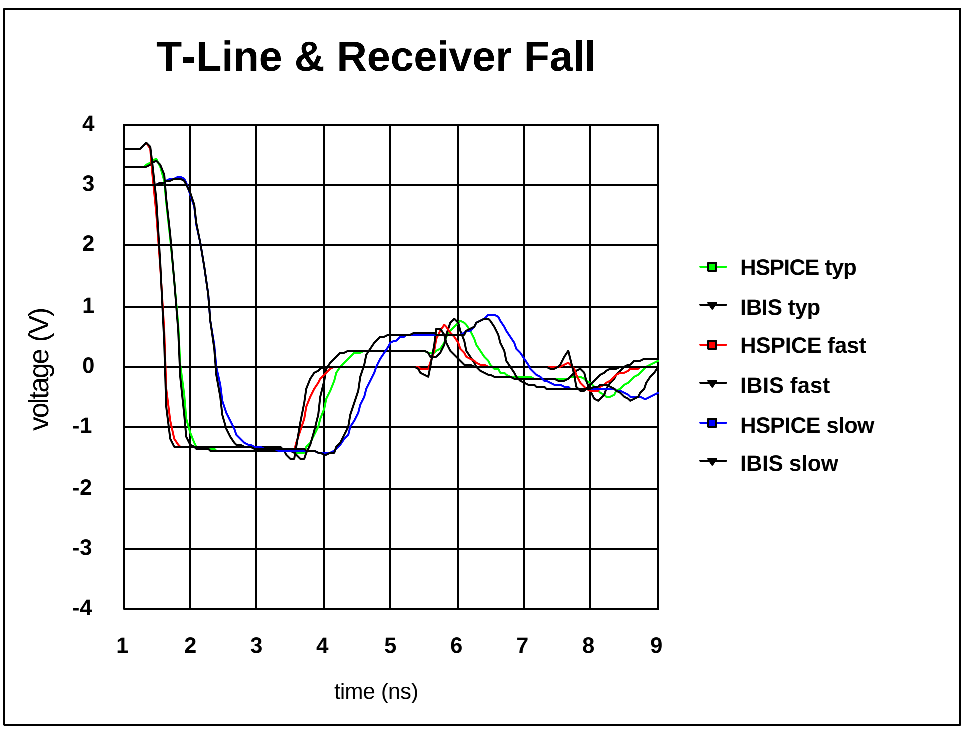


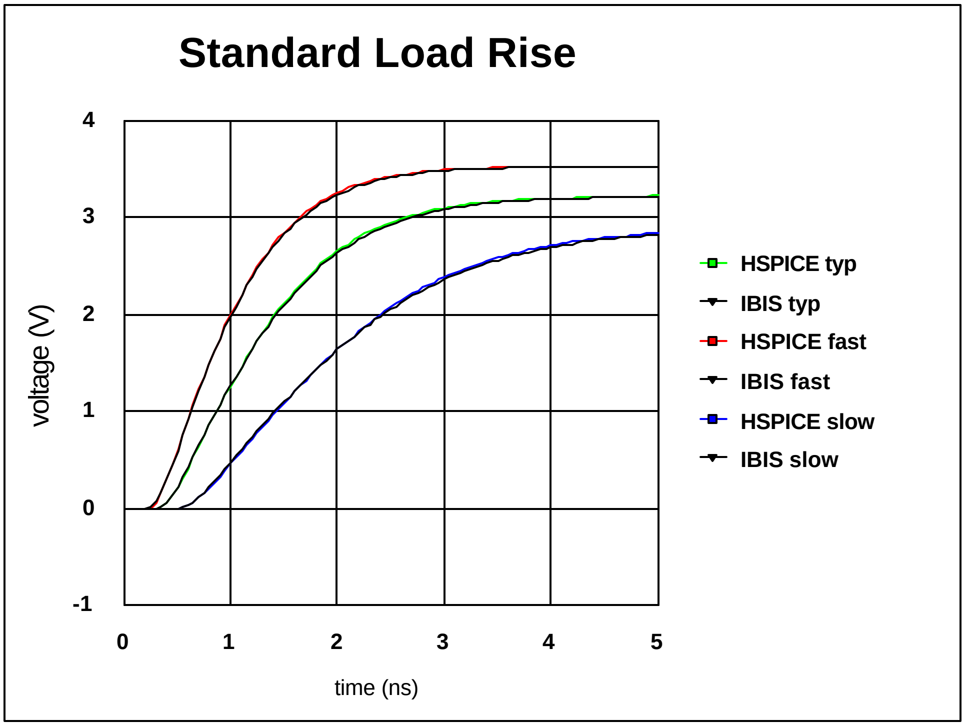


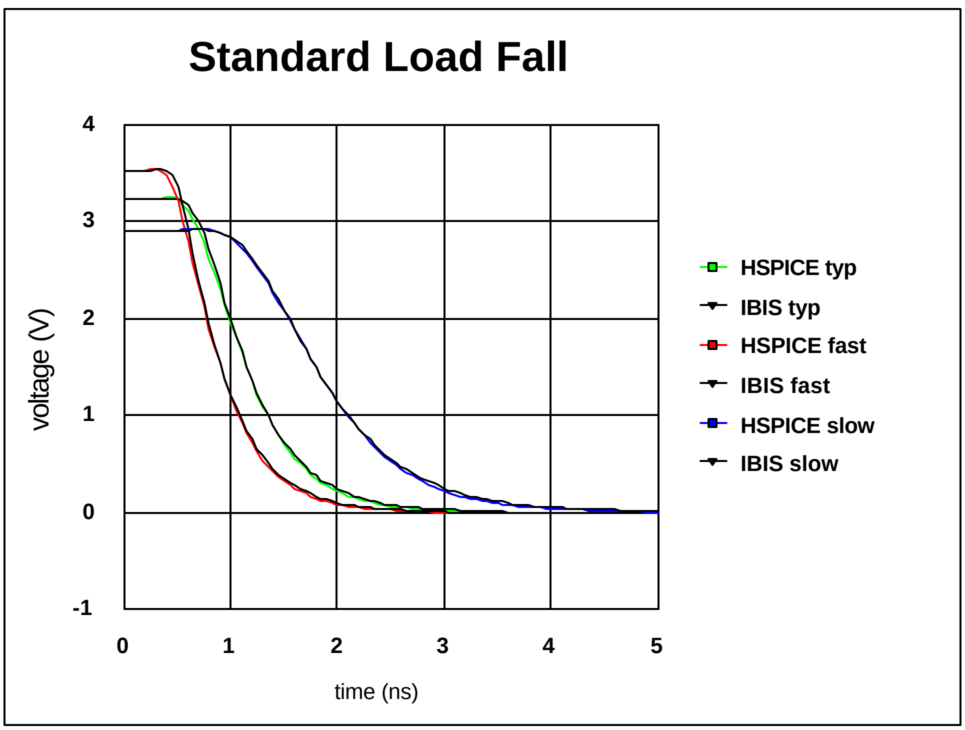

Open T-Line Rise
voltage (V)
7
6
5
4
3
2
1
0
-1
1
2
3
4
5
6
7
8
9
time (ns)
HSPICE typ
IBIS typ
HSPICE fast
IBIS fast
HSPICE slow
IBIS slow


Open T-Line Fall
voltage (V)
4
3
2
1
0
-1
-2
-3
-4
1
2
3
4
5
6
7
8
9
time (ns)
HSPICE typ
IBIS typ
HSPICE fast
IBIS fast
HSPICE slow
IBIS slow


T-Line & Receiver Rise
voltage (V)
7
6
5
4
3
2
1
0
-1
1 2 3 4 5 6 7 8 9
time (ns)
HSPICE typ
IBIS typ
HSPICE fast
IBIS fast
HSPICE slow
IBIS slow


T-Line & Receiver Fall
voltage (V)
4
3
2
1
0
-1
-2
-3
-4
1 2 3 4 5 6 7 8 9
time (ns)
HSPICE typ
IBIS typ
HSPICE fast
IBIS fast
HSPICE slow
IBIS slow


Standard Load Rise
voltage (V)
4
3
2
1
0
-1
0
1
2
3
4
5
time (ns)
HSPICE typ
IBIS typ
HSPICE fast
IBIS fast
HSPICE slow
IBIS slow


Standard Load Fall
voltage (V)
4
3
2
1
0
-1
0
1
2
3
4
5
time (ns)
HSPICE typ
IBIS typ
HSPICE fast
IBIS fast
HSPICE slow
IBIS slow

3.2 Figures of Merit

Table 5: IBIS vs. HSPICE Figures of Merit

Measurement	Overlay Fast	Overlay Typ	Overlay Slow
50 Ω to GND	99.79	99.78	99.71
50 Ω to VDD	99.70	99.67	99.70
Open T-line rising	98.96	98.61	98.84
Open T-line falling	98.90	98.25	98.88
T-Line and receiver rising	98.96	98.94	99.36
T-Line and receiver falling	97.62	98.36	97.27
Standard load rising	99.79	99.84	99.65
Standard load falling	99.76	99.74	99.72

3.3 Discrepancies

The only discrepancy worth noting in the IBIS vs. HSPICE correlation is the transmission line and receiver falling waveforms. Since I get good correlation on the rising waveforms, I suspect that I am seeing some charge storage capacitance that is not correctly modeled in IBIS when I turn on the ESD diode.

4. Component Datasheet Correlation

Table 6: Datasheet Capacitance Correlation

		Min	Typ	Max	Units
Cin	Datasheet	5	N/A	7	pF
	DUT	N/A	2.6	N/A	pF
	HSPICE	2.3	2.9	3.8	pF
	IBIS	2.3	2.9	3.8	pF
Cout	Datasheet	7	N/A	9	pF
	DUT	N/A	6.5	N/A	pF
	HSPICE	5.5	7.4	9.3	pF
	IBIS	5.5	7.4	9.3	pF

Table 7: Datasheet Edge Rate Correlation

		Min	Typ	Max	Units
Dvdtr	Datasheet	N/A	N/A	N/A	V/ns
	DUT	N/A	5.5	N/A	V/ns
	HSPICE	2.9	4.1	5.4	V/ns
	IBIS	4.2	7.7	11	V/ns
Dvdtf	Datasheet	N/A	N/A	N/A	V/ns
	DUT	N/A	8.2	N/A	V/ns
	HSPICE	4.1	7.1	9.1	V/ns
	IBIS	4.2	8.6	14	V/ns

Table 8: Datasheet Output Impedance Correlation

		Min	Typ	Max	Units
Zoutr	Datasheet	N/A	N/A	N/A	Ω
	DUT	N/A	14	N/A	
	HSPICE	11	14	21	Ω
	IBIS	11	13	20	Ω
Zoutf	Datasheet	N/A	N/A	N/A	Ω
	DUT	N/A	8.0	N/A	
	HSPICE	7.7	8.6	12	Ω
	IBIS	7.3	8.1	11	Ω

The data in the HSPICE and IBIS rows represent the full range of the process, voltage, and temperature space, i.e. 3.0 – 3.6 V and 0 – 100 C.

The HSPICE die capacitances values came from a dc operating point analysis. The package capacitances came from the vendor’s packaging group.

Table 9: Capacitance Values

Parameter	Corner	Cdie	Cpkg	Cpin	units
Cin	Fast	2.0	0.3	2.3	pF
	Typ	2.4	0.5	2.9	pF
	Slow	2.7	1.1	3.8	pF
Cout	Fast	5.2	0.3	5.5	pF
	Typ	6.9	0.5	7.4	pF
	Slow	8.2	1.1	9.3	pF

5. Conclusions

The HSPICE and IBIS model data show excellent correlation to the actual component. It is my opinion that these model data are ready to be incorporated into the IBM model library.