

Status of the VHDL 1076.1 Language

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Ernst Christen
Analogy, Inc.



Outline

- Status of Standardization
- Requirements trace
- Future work

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Status of Standardization

- First ballot completed in fall 1997
 - Approved by voters, but many comments
- Ballot Resolution Committee has responded to balloter comments
 - Several language changes
- Second ballot completed in May 1998
 - Approved by voters
- Standardization material submitted to IEEE RevCom for September meeting, resubmitted for December meeting
 - Third ballot necessary

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- Third ballot completed in February 1999
 - Approved by voters
- Standardization material resubmitted for March 1999 RevCom meeting
- IEEE Std. 1076.1-1999 approved on March 17, 1999

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Requirements Trace

- DO1 Design objectives must ensure reasonable degree of portability without putting restrictions on implementations
- Reliance on mathematical foundation
 - Careful definitions to yield the same simulation results in the limit
 - Tolerance parameters (which are dependent on algorithms) outside the language

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DO2 Should support non-electrical and mixed discipline systems

- Natures to specify physical discipline (energy domain)
- Simultaneous statements independent of natures

DO3 Must be a superset of VHDL 1076-1993

- Exceptions:
 - wait for now; -- use wait for time'(now);
 - wait for s'last_event; -- use wait for time'(s'last_event);
 - write(L, now); -- use write(L, real'(now));
 - write(L, s'last_event); -- use write(L, real'(s'last_event));

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VHDL 1076.1 Language Status

- DO4 Must support time domain simulation of lumped electrical systems**
- Complete specification of initialization
 - Complete specification of simulation cycle
- DO5 Re-use existing syntax where possible**
- Emphasis is on syntactic structure, not on syntax details
 - Created new syntactic structures only when necessary
 - Branch quantity, source quantity declaration
 - Nature declaration

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Page 7 of 27

VHDL 1076.1 Language Status

- DO6 Should support time domain simulation of lumped non-electrical systems**
- Complete specification of initialization
 - Complete specification of simulation cycle

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Page 8 of 27

VHDL 1076.1 Language Status

- DO7 Must support small-signal frequency domain analysis of lumped electrical systems**
- DO8 Should support small-signal frequency domain analysis of lumped non-electrical systems**
- Spectral source quantities
 - Complete specification of small-signal model
 - Complete specification of frequency domain calculation
 - Supports only analog portion of design

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Page 9 of 27

VHDL 1076.1 Language Status

- DO7b Desirable to support large-signal frequency domain analysis of lumped electrical systems**
- DO8b Desirable to support large-signal frequency domain analysis of lumped non-electrical systems**
- There is no general large-signal frequency domain algorithm
 - Language definition supports at least FFT
 - Language definition should not prevent Harmonic balance

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Page 10 of 27

VHDL 1076.1 Language Status

- DO9 Must support noise modeling and simulation**
- Noise source quantities
 - Complete specification of small-signal model
 - Complete specification of noise calculation
- DO9b Should not be restrictive to other types of analyses**
- We are not aware of any such restrictions due to the language definition

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Page 11 of 27

VHDL 1076.1 Language Status

- DO10 Must provide interaction mechanism between analog and digital**
- The name of a quantity can appear in an expression in a process
 - The name of a signal can appear in an expression in a simultaneous statement
 - Q'above(E)
 - Break statement, S'Ramp, S'Slew
 - User-written conversion models
- DO11 Basic A/D and D/A mechanisms must not be dependent on VHDL foreign interface**
- Complete specification of A/D and D/A interaction

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Page 12 of 27

VHDL 1076.1 Language Status

- DO12** A/D and D/A interface should be user customizable
- Conversion models are user-defined
 - User has control over threshold value in Q'above(E)
- DO13** Must support structural composition of digital, analog and mixed systems
- DO14** Must support conservation law and signal flow semantics at analog interconnections
- Extended port list to support signal ports, terminal ports and quantity ports
 - Defined semantics of association elements involving two terminals or two quantities

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Page 13 of 27

VHDL 1076.1 Language Status

- DO15** Should provide migration path for SPICE libraries and netlists
- Documented in white paper
 - Demonstrated by published examples
- DO16** Desirable to support conditional netlists
- VHDL'93 construct:
if condition generate
- DO17** Desirable to support regular structures of instances, e.g. two-dimensional array
- VHDL'93 construct:
for parameter_specification generate

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Page 14 of 27

VHDL 1076.1 Language Status

- DO18** Must support analog behavior specification by equations and sequentially
- Simple simultaneous statement, together with simultaneous if statement and simultaneous case statement
 - Simultaneous procedural statement
- DO19** Must support explicit and implicit equations
- Simple simultaneous statement is of the form
expression == expression ;
and supports, e.g., q == f(q)

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Page 15 of 27

VHDL 1076.1 Language Status

- DO20** Must support mixed structural/behavioral specification of a design entity
- Definition of simultaneous statements and concurrent statements as architecture statements
 - No restrictions on their use
- DO21** Must provide mechanism to access quantities inside a component that are not associated with terminals
- Two main purposes:
 - current-controlled sources
 - hierarchical summing of power
 - Quantity ports

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Page 16 of 27

VHDL 1076.1 Language Status

- DO22** Must support parameterized models
- VHDL'93 generics
- 22a)** Desirable to support dynamic parameters
- Quantity ports
- 22b)** Must be able to distinguish between unspecified and defaulted parameters
- Requirement comes from SPICE model parameters that must be computed if no value is provided by user
 - Problem can be addressed by defaulting such parameters to a special value, e.g. REAL'LOW

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Page 17 of 27

VHDL 1076.1 Language Status

- DO23** Must support time dependent and frequency dependent descriptions
- Overloaded function NOW to return real value
 - NOW can appear in any expression
 - Defined function FREQUENCY, can appear in expressions defining source quantities
- DO24** Must support discontinuous behavior
- The name of a signal can appear in a simultaneous statement
 - Break statement to announce discontinuity
 - S'Ramp, S'Slew

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799

Page 18 of 27

VHDL 1076.1 Language Status

- DO25** Minimum time resolution of VHDL type time must not limit maximum simulation time
- Defined continuous time and its correspondence to discrete time
 - Implementations can change the resolution limit without affecting the correspondence
- DO26** Must provide time derivative operator
- Q'Dot
- DO27** Must provide predefined mathematical functions
- Available in VHDL 1076.2 math package

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Page 19 of 27

VHDL 1076.1 Language Status

- DO28** Should support piecewise defined behavior
- Simultaneous if statement
 - Simultaneous case statement
 - If and case statements in simultaneous procedural statement
- DO29** Should provide time integral operator
- Q'Integ
- DO30** Should support annotation of physical units
- Demonstrated use of user-defined attributes for this purpose
- DO31** Desirable to support dimensional analysis
- Not supported, requires changes to type system

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Page 20 of 27

VHDL 1076.1 Language Status

- DO32** Should provide default conversion between analog and digital connection points
- Decided to postpone for next revision of the language after long discussions
- DO33** Must provide user-customizable threshold function
- Q'above(E), where E is defined by the model writer

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Page 21 of 27

VHDL 1076.1 Language Status

- DO34** Must allow a process to read an analog value; must allow a process to be sensitive to an analog value
- The name of a quantity can appear in an expression in a process
 - Since Q'above(E) is a signal, a process can be sensitive to it
- DO35** Analog model must be able to read digital signal; must allow an analog model to be sensitive to a signal
- The name of a signal can appear in an expression in a simultaneous statement
 - Break statement, S'Ramp, S'Slew

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Page 22 of 27

VHDL 1076.1 Language Status

- DO36** Should handle discontinuity caused by digital signal appearing in an equation
- S'Ramp
 - S'Slew
 - Break statement
- DO37** Must not specify algorithm for analog kernel
- Reliance on mathematical foundation
- DO38** Must specify mixed analog/digital simulation cycle
- Complete specification of initialization
 - Complete specification of simulation cycle

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Page 23 of 27

VHDL 1076.1 Language Status

- DO39** Must support user-defined initial conditions
- Break statement
- DO40** Should provide communication mechanism between analog model and analog kernel
- Limit step specification, to specify an upper limit for the next time step taken by the analog kernel

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Page 24 of 27

Future Work

Configurable conversion models

- **Associations of:**
 - terminal <-> signal, with either as formal
 - quantity <-> signal, with either as formal
 - terminal <-> quantity, with either as formal
- **Analysis of basic issues exists, but maybe there are missing requirements**
- **Need to study capabilities of Verilog-AMS connect statement**
- **Desirable to use VHDL configurations**

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Page 25 of 27

Frequency Domain Modeling

- **Support frequency domain modeling beyond frequency-dependent sources**
 - Needed for RF and microwave simulation
 - Requires completely different set of algorithms
 - Definitional difficulties
 - VHDL-RF study group
- **Support frequency domain analysis of event-driven portion of design**
 - No algorithms available for the general case
 - Restriction to multi-rate clocking schemes possible, but requires additional semantics in the language

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Page 26 of 27

Dimensional Analysis

- **In most non-electrical environments a multitude of units are in common use for each dimension**
 - e.g. length: m, cm, mm, km, inch, yard, mile, light year
- **Analysis shows that complete dimensional analysis is incompatible with VHDL type system**
- **Can (should) we do a partial solution that only supports “dimensional conversion” for generics?**

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Page 27 of 27